RoHS

COMPLIANT

HALOGEN

FREE

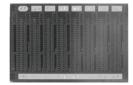
GREEN

(5-2008)



Wire Bondable Thin Film Resistor Arrays





Product may not be to scale

The CLA and CLB resistor arrays are the hybrid equivalent to the eight resistor common connection and isolated networks available in sips or dips. The resistors are spaced on 0.010" centers resulting in minimal space requirements.

These chips are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CLA and CLBs are 100 % electrically tested and visually inspected to MIL-STD-883.

FEATURES

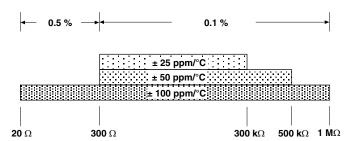
- · Wire bondable
- Up to 12 equal value resistors
- For case see Part Dimensions table
- Resistance range: 20 Ω to 1 M Ω
- Excellent TCR tracking
- Resistor material: tantalum nitride, self-passivating
- Oxidized silicon substrate for good power dissipation
- · Custom values and pad geometries available
- Moisture resistant
- Material categorization: for definitions of compliance please see <u>www.vishav.com/doc?99912</u>

APPLICATIONS

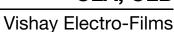
The CLA and CLB thin film resistor arrays are designed for hybrid packages requiring up to twelve resistors of the same resistance value and tolerance, as well as excellent TCR tracking. For such hybrids, they afford great savings in cost and space.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES, AND TOLERANCES				
PARAMETER	VALUE	UNIT		
Total Resistance Range	20 to 1M	Ω		
Standard Tolerances	± 0.1, ± 0.5	%		
TCR	± 25, ± 50, ± 100	ppm/°C		

Tightest Standard Tolerance Available

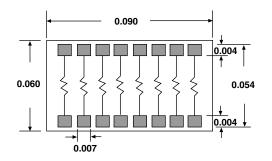


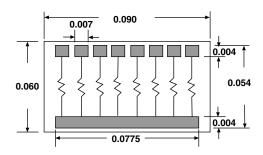
STANDARD ELECTRICAL SPECIFICATIONS				
PARAMETER	VALUE	UNIT		
TCR Tracking Spread	± 5	ppm/°C		
Noise, MIL-STD-202, Method 308 100 Ω to 250 k Ω	-35 typ. -20 typ.	dB		
$<$ 100 Ω or $>$ 251 k Ω Moisture Resistance, MIL-STD-202, Method 106	± 0.5 max. Δ <i>R</i> / <i>R</i>	%		
Stability, 1000 h, +125 °C, 25 mW Absolute Ratio	\pm 0.25 max. $\Delta R/R$ \pm 0.05 max. $\Delta R/R$	%		
Operating Temperature Range	-55 to +125	°C		
Thermal Shock, MIL-STD-202 Method 107, Test Condition F	± 0.1 max. Δ <i>R/R</i>	%		
High Temperature Exposure, ± 150 °C, 100 h	± 0.2 max. ΔR/R	%		
Dielectric Voltage Breakdown	200	V		
Insulation Resistance	10 ¹² min.	Ω		
Operating Voltage	100	V		
DC Power Rating at +70 °C (Derated to Zero at 175 °C)	0.050 per resistor	W		
5 x Rated Power Short-Time Overload, +25 °C, 5 s	± 0.1 % max. Δ <i>R/R</i>	%		





DIMENSIONS in inches



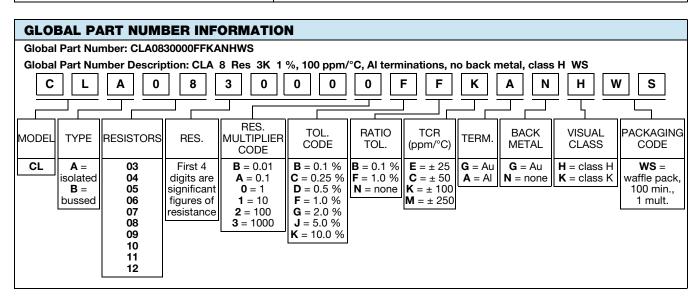


CLA 8 Cell

CLB 8 Cell

DIMENSIONS in inches					
# OF RES.	03	04	06	08	12
CLA	0.060 x 0.060 ± 0.003	$0.050 \times 0.060 \pm 0.003$	0.069 x 0.060 ± 0.003	0.090 x 0.060 ± 0.003	0.130 x 0.060 ± 0.003
CLB	0.060 x 0.060 ± 0.003	$0.050 \times 0.060 \pm 0.003$	0.069 x 0.060 ± 0.003	0.090 x 0.060 ± 0.003	$0.130 \times 0.060 \pm 0.003$

MECHANICAL SPECIFICATIONS			
PARAMETER			
Chip Size	See Dimensions table above		
Chip Thickness	0.010" ± 0.002" (0.254 mm ± 0.05 mm)		
Chip Substrate Material	Oxidized silicon, 10 kÅ minimum SiO2		
Resistor Material	Tantalum nitride, self-passivating		
Bonding Pads	0.004" x 0.007" (0.10 mm x 0.178 mm)		
Number of Top Pads	CLA - 16 CLB - 9		
Pad Material	10 kÅ minimum aluminum		
Backing	None, lapped semiconductor silicon		





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