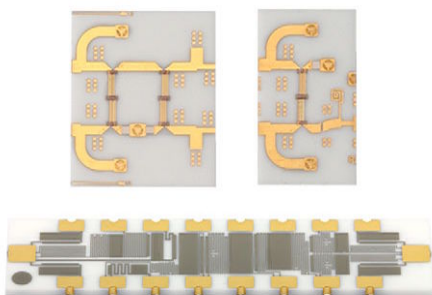


## Custom Substrates - Metal Via / Multilayer / Lumped Element



### FEATURES

- Plated or filled via technology
- Multilayer and overcoat patterning
- Lumped element custom substrates
- $\text{Al}_2\text{O}_3$ , AlN, and BeO substrate drilling and shaping
- TaN and NiCr resistor films
- Metallization on 1, 2, or 4 surfaces
- Various substrate materials
- Sputtered / plated metal systems
- Custom sizes from 0.020" x 0.020" to 4.000" x 4.000"
- Quick delivery available

### APPLICATIONS

Vishay EFI custom interconnect substrates are used in military, aerospace, hybrid circuit, telecommunications, microwave, and industrial applications. These custom interconnect substrates are manufactured to be used in heat transfer connectors, top to bottom connectors, and RF / microwave designs. Surface connections can be made by plated thru-holes, edge wraps, or filled via technologies. Custom cutouts of various sizes and shapes can also be created and used to fit into almost any size and shape. The custom interconnect substrates are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The custom interconnect substrates are 100 % electrically tested (when applicable) and visually inspected to MIL-STD-883, method 2032 class H or K.

### THIN FILM DESIGN GUIDELINES

For further detail, please reference document: Thin Film Design Guide for Custom Substrates ([www.vishay.com/doc?49109](http://www.vishay.com/doc?49109))

### SUBSTRATE MATERIALS

For substrate materials and their properties, please reference datasheet: SPF1 ([www.vishay.com/doc?61105](http://www.vishay.com/doc?61105))

### METAL SYSTEM AND CONDUCTOR PATTERNING

For metal patterning design guidelines please reference datasheet: SPF2 ([www.vishay.com/doc?61110](http://www.vishay.com/doc?61110))

### THIN FILM RESISTORS

For thin film resistors and their properties and design guidelines, please reference datasheet: PSS ([www.vishay.com/doc?61111](http://www.vishay.com/doc?61111))

### PROTECTIVE COATINGS

For protective coatings or overcoat options and their properties and design guidelines, please reference datasheet PSS: PSS ([www.vishay.com/doc?61111](http://www.vishay.com/doc?61111))

## FRONT TO BACK CONTINUITY

For designs requiring metal or electrical connection from the top to the bottom of the substrate, metal via connections will be used. Metalized Edge Wraps are chosen for applications where soldering to the side of the substrate is desired for connection to the PCB or module design. Plated thru-holes are used for applications where the module design may require alignment or soldering pins to be inserted into the holes. Filled vias are used for applications where the strongest electrical connection is needed or preventing solder migration to the backside. See Fig. 1 below for edge wrap, plated thru-hole, and filled via pictorial representation.

| <b>METALLIZED EDGE WRAPS</b>                    |                                  |
|-------------------------------------------------|----------------------------------|
| Min. distance from wrap edge to pattern edge    | 0.005"                           |
| Min. tolerance from wrap center to pattern edge | ± 0.002"                         |
| Wrap diameter (as measured from exit side)      | 0.8 to 2.0 x substrate thickness |

| <b>PLATED THRU-HOLES</b>                        |                                  |
|-------------------------------------------------|----------------------------------|
| Min. distance from hole edge to pattern edge    | 0.005"                           |
| Min. tolerance from hole center to pattern edge | ± 0.002"                         |
| Hole diameter (as measured from exit side)      | 0.8 to 2.0 x substrate thickness |
| Min. hole center to hole center spacing         | 2 x hole diameter                |

| <b>FILLED VIAS</b>                                  |                                 |
|-----------------------------------------------------|---------------------------------|
| Min. distance from via edge to pattern edge         | 0.0025"                         |
| Min. tolerance from via center to pattern edge      | ± 0.002"                        |
| Min. via center to via center spacing               | 2 x via diameter                |
| Preferred via diameter (as measured from exit side) | 0.8 x substrate thickness       |
| Via diameter range (as measured from exit side)     | 0.6 - 1.5 x substrate thickness |
| Min. via diameter                                   | 0.007"                          |
| Max. via diameter                                   | 0.040"                          |

### Note

- These rules apply to the non-vented via side

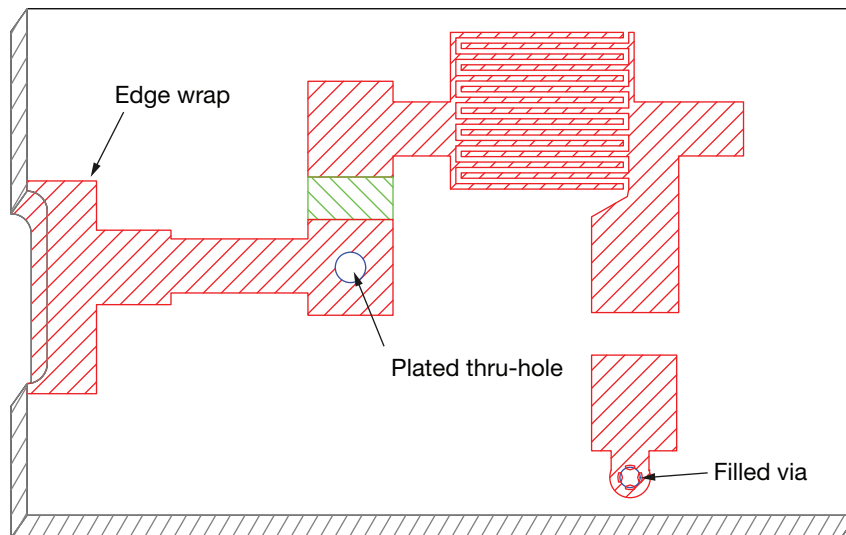


Fig. 1

**FILLED VIA VENT NOTES**

|                                                  |        |
|--------------------------------------------------|--------|
| Min. distance from via vent edge to pattern edge | 0.004" |
|--------------------------------------------------|--------|

**Note**

- Via vents are required on one side of the substrate if metals are plated
- See Fig. 2 for via vent pattern example

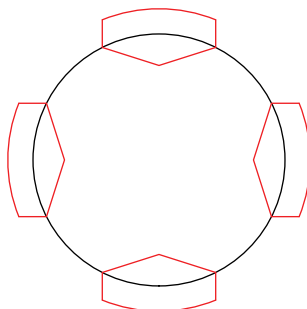


Fig. 2

**SHAPES AND CUT-OUTS**

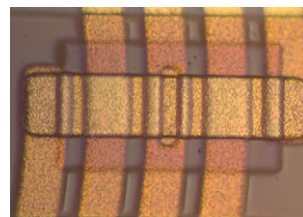
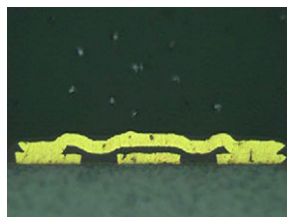
Many circuit designs require custom substrates with different shapes and holes cutout of the parts. These include cutting out material internal and external to the overall part size and shape.


**PART SHAPE / CUT-OUTS**

|                                                  |          |
|--------------------------------------------------|----------|
| Min. distance from cut-out edge to pattern edge  | 0.003"   |
| Min. tolerance from cut-out edge to pattern edge | ± 0.002" |
| Min. tolerance of cut-out feature                | ± 0.003" |
| Min. distance between cut-outs                   | 0.050"   |

## MULTILAYER AND AIR BRIDGE

For certain complex designs multiple layers of metal and / or interlevel dielectrics are required. Vishay Electro-Films has developed precision patterning and layering techniques where  $\pm 0.0001"$  pattern tolerance and  $\pm 0.0005"$  layer to layer alignment is achievable.



For Multilayer designs that require an interlevel dielectric the following two choice are currently available:

| DIELECTRIC                     | TYPICAL THICKNESS    | PATTERN TOLERANCE | DIELECTRIC CONSTANT |
|--------------------------------|----------------------|-------------------|---------------------|
| Silicon nitride <sup>(1)</sup> | 4000 Å to 6000 Å     | $\pm 0.002"$      | -                   |
| Polyimide                      | 50 000 Å to 80 000 Å | $\pm 0.002"$      | 3.2 at 1 MHz        |

### Note

<sup>(1)</sup> Silicon nitride can also be used to integrate a capacitive element to the design if needed

In applications where large couplers and cross-metal patterning are needed, air bridges can be used to connect different metal patterns using polyimide supported bridges. These bridges require several design guidelines for layering the base metal, polyimide, and bridge metal into the optimum air bridge design.

Fig. 3 can be used as a guideline for a typical large coupler / air bridge set-up. The dimensions listed in the bubble detail picture are considered minimums for any design. For more specific design layout guidelines, contact the factory for more information.

| MULTI-LEVEL CROSSOVER DESIGN PARAMETERS |                         |                                                                  |                                                      |
|-----------------------------------------|-------------------------|------------------------------------------------------------------|------------------------------------------------------|
| PARAMETER                               |                         | MINIMUM VALUE<br>(in $\mu\text{m}$ )                             | COMMENTS                                             |
| Dimension                               | Crossover thickness     | 0.0001 (2.5)                                                     | Minimum                                              |
| A                                       | Crossover width         | 0.001 (25)                                                       | 0.0001 in crossover to conductor pullback            |
| B                                       | Crossover length        | 0.003 (75)                                                       | Minimum                                              |
| C / D                                   | Insulator dimension     | Length: 0.0015 (37.5)<br>Width: 0.003 (76)                       | 0.0025 (63)<br>insulator-to-conductor overlap        |
|                                         | Insulator material      |                                                                  | Polyimide                                            |
| E / F                                   | Encapsulation dimension | Crossover width: +0.0015 (37.5)<br>Crossover length: +0.003 (76) | These values are added to the<br>insulator dimension |
|                                         | Encapsulation material  |                                                                  | Polyimide                                            |

### Note

- These rules apply to the non-vented via side

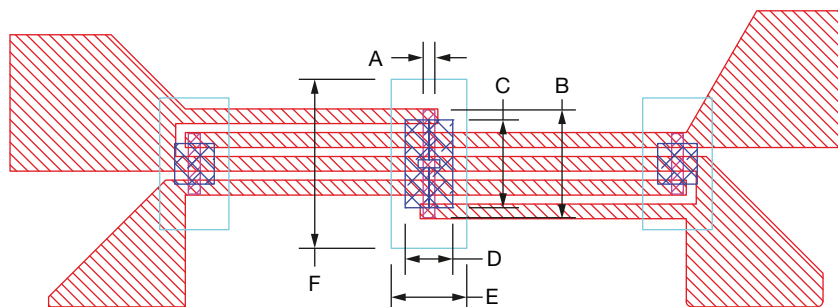


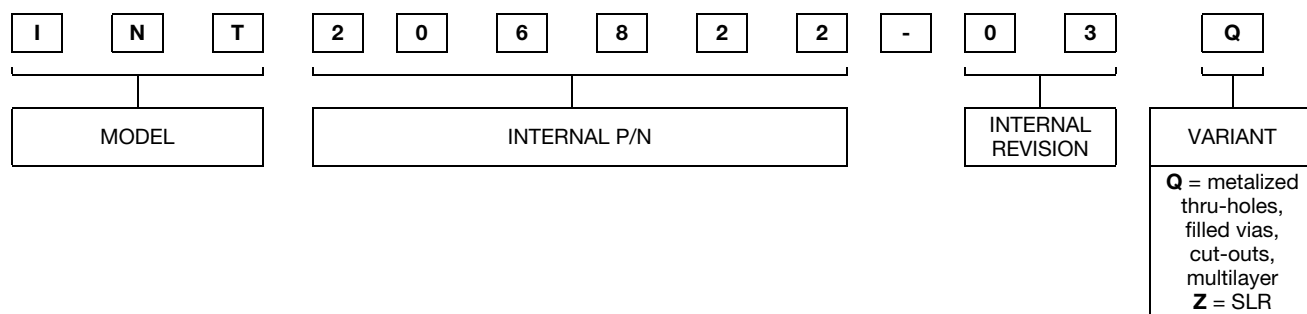
Fig. 3



## GLOBAL PART NUMBER INFORMATION

Custom Global Part Number: INT206822-03Q

Custom Global Part Number Description: interconnect custom 206822-03Q



### Note

- Z = SLR, see separate SLR datasheet ([www.vishay.com/doc?61068](http://www.vishay.com/doc?61068))

## CONTACT INFORMATION

For design assistance, contact: [efi@vishay.com](mailto:efi@vishay.com)



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