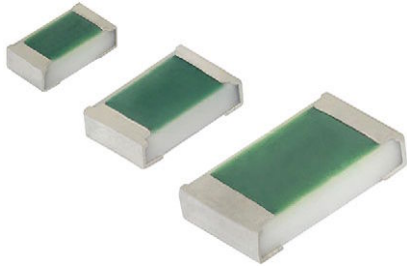


Hi-Rel Thin Film Chip Resistors


 HALOGEN
FREE

FEATURES

- High-reliability product
- ESA approved to ESCC 4001/029
- Advanced thin film technology
- SnPb termination plating, minimum 6 % Pb
- Single Lot Date Code
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Aerospace
- Avionics
- Military

TNPS ESCC high-reliability thin film chip resistors are the premium choice for design and manufacture of equipment where a mature technology and proven reliability are of utmost importance. They are regularly used in communication and research satellites and fit equally well into aircraft and military electronic systems.

Approval of the TNPS ESCC products is granted by the European Space Components Coordination and registered in the ESCC Qualified Parts List, REP005.

TECHNICAL SPECIFICATIONS			
DESCRIPTION	TNPS0603 ESCC	TNPS0805 ESCC	TNPS1206 ESCC
DIN size	0603	0805	1206
Metric size code (EN/CECC style)	RR1608M	RR2012M	RR3216M
Resistance range	10 Ω to 221 kΩ	10 Ω to 422 kΩ	10 Ω to 1 MΩ
Resistance tolerance	± 1 %; ± 0.5 %; ± 0.1 %		
Temperature coefficient	± 50 ppm/K; ± 25 ppm/K; ± 15 ppm/K		
Rated dissipation P_{70}	0.1 W	0.125 W	0.25 W
Operating voltage, U_{max} , AC _{RMS} or DC	75 V	150 V	200 V
Permissible film temperature, $\vartheta_{F max}$.	125 °C		
Operating temperature range	-55 °C to 125 °C		
Max. resistance change at P_{70} , $ \Delta R $ max., after:			
1000 h	≤ (0.05 % R + 10 mΩ)		
2000 h	≤ (0.1 % R + 20 mΩ)		
Permissible voltage against ambient (insulation)	100 V	200 V	300 V
Storage temperature range	-55 °C to +125 °C		

Note

- These resistors do not feature a limited lifetime when operated within the permissible limits. However, resistance value drift increasing over operating time may result in exceeding a limit acceptable to the specific application, thereby establishing a functional lifetime



TEMPERATURE COEFFICIENT AND RESISTANCE RANGE				
TYPE / SIZE	TCR	TOLERANCE	RESISTANCE	E-SERIES
TNPS0603 ESCC	± 50 ppm/K	± 1 %	10 Ω to 221 kΩ	E96
	± 25 ppm/K	± 0.5 %		
	± 15 ppm/K	± 0.1 %		
TNPS0805 ESCC	± 50 ppm/K	± 1 %	10 Ω to 422 kΩ	
	± 25 ppm/K	± 0.5 %		
	± 15 ppm/K	± 0.1 %		
TNPS1206 ESCC	± 50 ppm/K	± 1 %	10 Ω to 1 MΩ	
	± 25 ppm/K	± 0.5 %		
	± 15 ppm/K	± 0.1 %		

Notes

- The listed combinations of TCR, tolerance and resistance range are a subset of those combinations approved to ESCC 4001/029
- Resistance values from other E-series than given are not permitted in ESCC 4001/029

PACKAGING						
TYPE / SIZE	CODE	QUANTITY ⁽¹⁾	PACKAGING STYLE	WIDTH	PITCH	PACKAGING DIMENSIONS
TNPS0603 ESCC TNPS0805 ESCC TNPS1206 ESCC	BX	≥ 100 to 499	Antistatic blister tape acc. IEC 60286-3, Type 2a ⁽³⁾	8 mm	4 mm	Box
		≥ 500 ⁽²⁾				Reel, Ø 180 mm / 7"
	LX	≤ 100	Matrix tray ⁽⁴⁾	-	4.2 mm	55 mm x 51 mm x 11 mm

Notes

- ⁽¹⁾ The minimum order quantity is 100 pieces, except for samples for Lot Validation Testing
- ⁽²⁾ The maximum reel capacity is 3000 pieces
- ⁽³⁾ The tape leader is extended to 500 mm cover tape, including 200 mm carrier tape with empty compartments
- ⁽⁴⁾ The matrix tray (waffle tray) packaging, code LX, is available only for samples for lot validation testing



PART NUMBER AND PRODUCT DESCRIPTION

PART NUMBER: TNPS08057502DEBX00

T N P S 0 8 0 5 7 5 0 2 D E B X 0 0

TYPE / SIZE TNPS0603 TNPS0805 TNPS1206	RESISTANCE 3 digit value 1 digit multiplier MULTIPLIER 9 = *10 ⁻¹ 0 = *10 ⁰ 1 = *10 ¹ 2 = *10 ² 3 = *10 ³ 4 = *10 ⁴	TOLERANCE F = ± 1 % D = ± 0.5 % B = ± 0.1 %	TCR H = ± 50 ppm/K E = ± 25 ppm/K X = ± 15 ppm/K	PACKAGING BX LX
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PRODUCT DESCRIPTION: TNPS0805 25 75K0 0.5 % BX ESCC 4001/029

TNPS0805	25	75K0	0.5 %	BX	ESCC 4001/029
TYPE / SIZE TNPS0603 TNPS0805 TNPS1206	TCR ± 50 ppm/K ± 25 ppm/K ± 15 ppm/K	RESISTANCE 33R2 = 33.2 Ω 75K0 = 75.0 kΩ	TOLERANCE ± 1 % ± 0.5 % ± 0.1 %	PACKAGING BX LX	SPECIFICATION ESCC 4001/029

Notes

- Products can be ordered using either the PART NUMBER or the PRODUCT DESCRIPTION
- Products within a packaging unit are Single Lot Date Code

ESCC 4001/029 COMPONENT NUMBER AND ELECTRICAL CHARACTERISTICS

Example of the component number and electrical characteristics for a resistor: TNPS0805 25 75K0 0.5 % ESCC 4001/029

400102902 7502D2

The elements used in the component number have the following meaning:

4001029	Detail specification number, ESCC 4001/029
02	Type variant (Size):
	01 0603
	02 0805
	03 1206

The elements used in the electrical characteristics number have the following meaning:

7502	Resistance acc. IEC 60062, four-character code system
D	Tolerance on rated resistance acc. IEC 60062
2	Temperature coefficient of resistance:
	3 ± 50 ppm/K
	2 ± 25 ppm/K
	1 ± 15 ppm/K



DESCRIPTION

Production is strictly controlled and follows an extensive set of instructions established for reproducibility. A homogeneous film of metal alloy is deposited on a high grade ceramic substrate (Al₂O₃) and conditioned to achieve the desired temperature coefficient. Specially designed inner contacts are deposited on both sides. A special laser is used to achieve the target value by smoothly fine trimming the resistive layer without damaging the ceramics. A further conditioning is applied in order to stabilize the trimming result. The resistor elements are covered by a protective coating designed for electrical, mechanical, and climatic protection. The terminations receive a final SnPb plating, controlled for a minimum lead content of 6 %. The result of the determined production is verified by an extensive testing procedure performed on 100 % of the individual chip resistors. Only accepted products are placed into a special matrix case packaging or into antistatic blister tape in accordance with **IEC 60286-3 (1), type 2a**.

Products within a packaging unit are from the same production lot and carry the same date code.

ASSEMBLY

The resistors are suitable for processing on automatic SMD assembly systems. They are suitable for automatic soldering using wave, reflow, or vapor phase as shown in **IEC 61760-1 (1)**. Solderability is specified for 2 years after production. The permitted storage time is 20 years.

The encapsulation is resistant to all cleaning solvents commonly used in the electronics industry, including alcohols, esters, and aqueous solutions. The suitability of conformal coatings, potting compounds, and their processes, if applied, shall be qualified by appropriate means to ensure the long-term stability of the whole system.

MATERIALS

Vishay acknowledges the IEC 62474 (1), Material Declaration for Products of and for the Electrotechnical Industry, and complies with the reporting requirements on declarable substances given therein (2).

Vishay acknowledges the REACH regulation (1907/2006/EC) and the related list of substances of very high concern (SVHC) (3) for its supply chain.

Except for the intentionally added lead (Pb) in the termination finish, the products do not contain any of the declarable substances as per IEC 62474, or as per the SVHC list, see www.vishay.com/how/leadfree.

Vishay pursues the elimination of conflict minerals from its supply chain, see the Conflict Minerals Policy at www.vishay.com/doc?49037.

APPROVALS

The resistors are approved to **ESCC 4001/029**. Conformity is indicated by the **ESCC Qualified Components** logo on the package label. Approval is granted by the European Space Components Coordination and registered in the ESCC Qualified Parts List, REP005.

The detail specification **ESCC 4001/029** has been established after successful completion of an **Evaluation Test Programme** according to **ESCC 2264000**.

SCREENING TESTS

These products are subjected to a screening test according to the ruling of the generic specification **ESCC 4001** and the detail specification **ESCC 4001/029**.

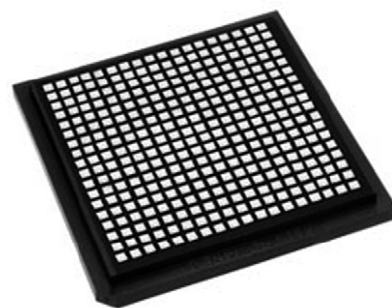
The production is succeeded by production test sequences for resistance, plating properties, solderability, and dimensions. This sequence is followed by screening tests for overload, non-linearity, temperature coefficient, resistance at room temperature, and a visual inspection. A Certificate of Conformity provides summary information by reporting the numbers of rejects for each test or inspection.

LOT VALIDATION TESTS

Execution of Lot Validation Tests according to the ruling of **ESCC 4001** is available as a separate order item. This is to be combined with the dedicated order line for the required amount of samples, using packaging code "LX".

The applicable scope of the Lot Validation Tests, graduated to Group 1, Group 2, and Group 3 is illustrated further below with the number of samples required for each level.

Deliverable item to the Lot Validation Tests is the test report together with the used samples, shipped in waffle tray package.



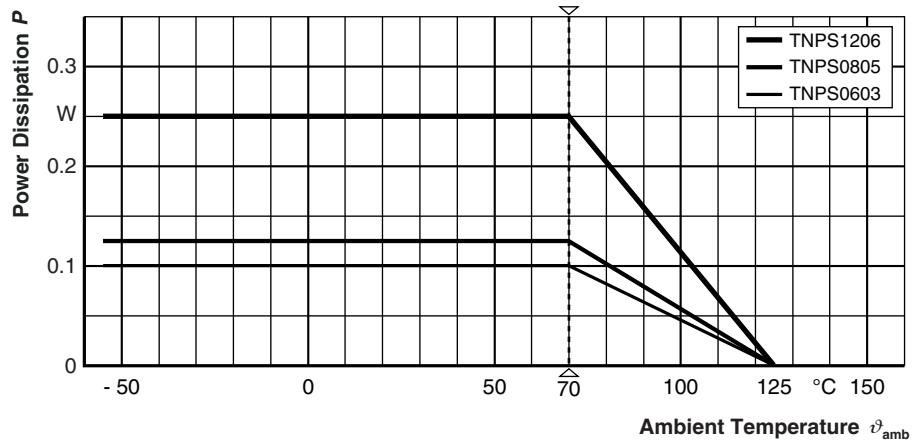
Waffle Tray

Notes

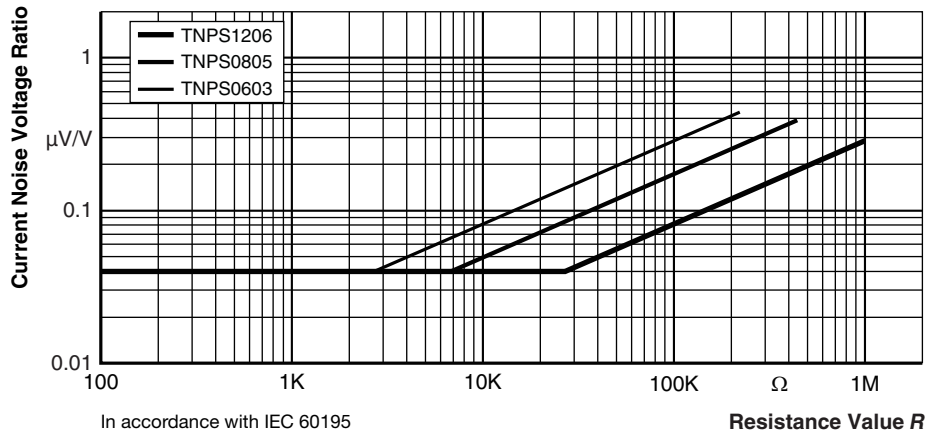
- (1) The quoted IEC standards are also released as EN standards with the same number and identical contents
- (2) The IEC 62474 list of declarable substances is maintained in a dedicated database, which is available at <http://std.iec.ch/iec62474>
- (3) The SVHC list is maintained by the European Chemical Agency (ECHA) and available at <http://echa.europa.eu/candidate-list-table>



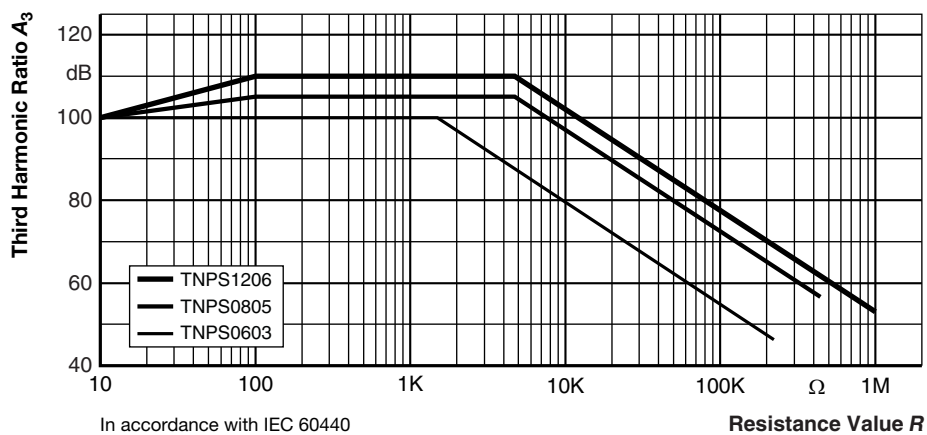
FUNCTIONAL PERFORMANCE



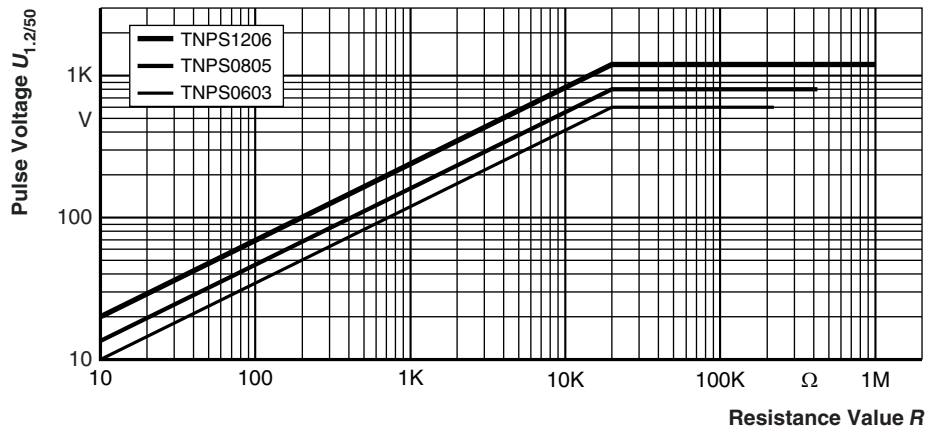
Derating



Current Noise Voltage Ratio

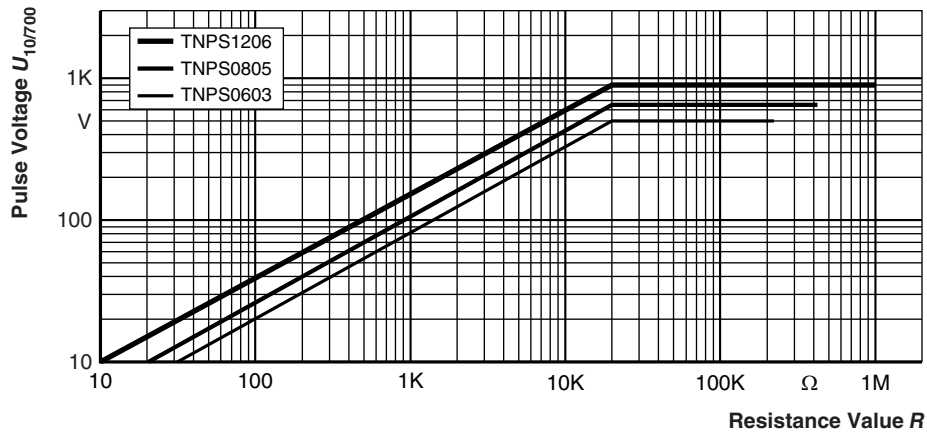


Non-Linearity - Third Harmonic Ratio A₃



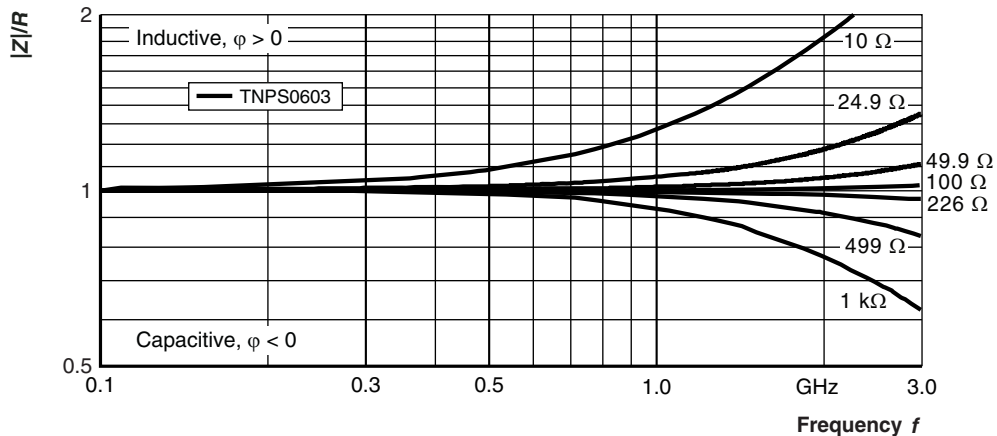
Pulse load rating in accordance with IEC 60115-1, 4.27; 1.2 μ s / 50 μ s;
5 pulses at 12 s intervals; for permissible resistance change 0.5 %

1.2 μ s / 50 μ s Pulse

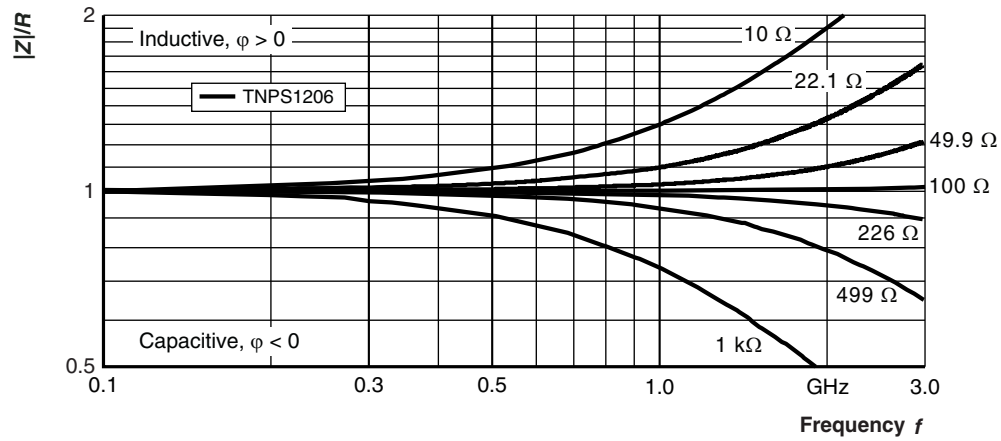
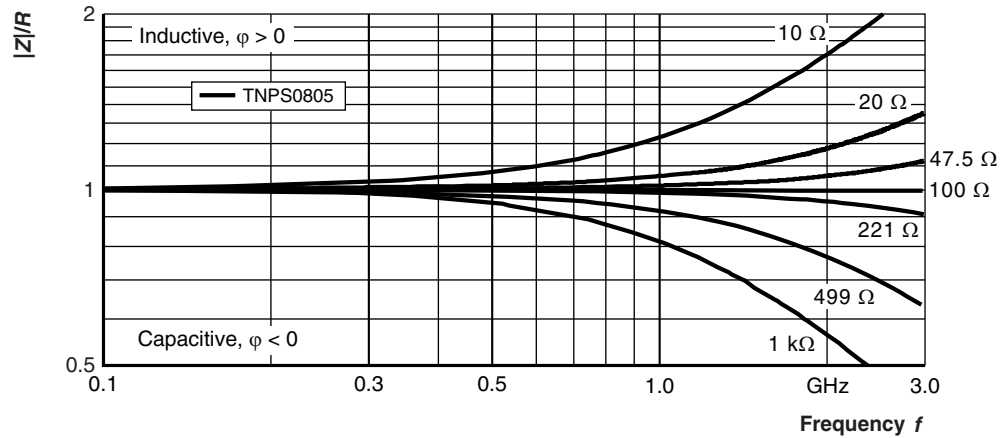


Pulse load rating in accordance with IEC 60115-1, 4.27; 10 μ s / 700 μ s;
10 pulses at 1 min intervals; for permissible resistance change 0.5 %

10 μ s / 700 μ s Pulse



RF-Behaviour





TESTS AND REQUIREMENTS

All tests are carried out in accordance with the following specifications:

ESCC 4001, generic specification, issue 5 (2019)

ESCC 4001/029, detail specification, issue 3 (2014)

The components are approved within the ESCC system. For the full test schedule refer to the documents listed above.

The tests are carried out in accordance with the stated specifications.

Unless otherwise specified the following standard atmospheric conditions apply:

Temperature: 15 °C to 35 °C

Relative humidity: 25 % to 75 %

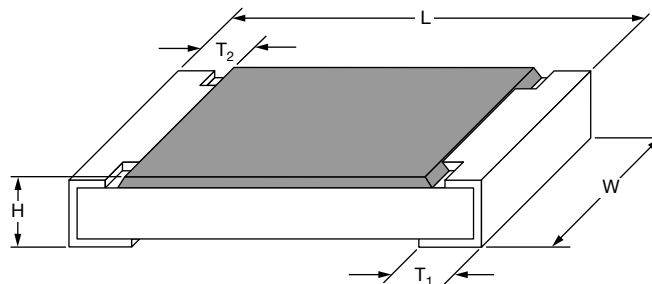
Air pressure: 86 kPa to 106 kPa (860 mbar to 1060 mbar)

The components are mounted for testing on printed-circuit boards in accordance with EN 60115-8, 2.4.2, unless otherwise specified.

TEST PROCEDURES AND REQUIREMENTS												
ESCC 4001 PARAGRAPH	ESCC 4001/029 PARAGRAPH	TEST	PROCEDURE	REQUIREMENTS PERMISSIBLE CHANGE (ΔR)								
			Stability for product types:									
			TNPS0603	10.0 Ω to 221 k Ω								
			TNPS0805	10.0 Ω to 422 k Ω								
			TNPS1206	10.0 Ω to 1.00 M Ω								
PRODUCTION CONTROL (CHART F2)												
8.3.2	2.5.1	Resistance	(22 \pm 3) °C	\pm 1 % R; \pm 0.5 % R; \pm 0.1 % R								
4.5	(ESCC 23500) 1.8.2	Plating - Thickness - Pb contents	X-ray fluorescence analysis	SnPb layer \geq 3 μ m \geq 6 % Pb								
8.14	(IEC 60068-2-20, Ta)	Solderability	Solder bath method; SnPb40; non-activated flux; (235 \pm 5) °C; (2 \pm 0.5) s	Good tinning (\geq 95 % covered); No visible damage; \pm (0.02 % R + 10 m Ω)								
8.6	1.6	Dimension check	-	-								
SCREENING TESTS (CHART F3)												
8.1	2.1.1.1 1.5	Overload	$U = \sqrt{k \times P_{70} \times R}$ <table border="1"> <thead> <tr> <th>Style</th> <th>k</th> </tr> </thead> <tbody> <tr> <td>0603</td> <td>30</td> </tr> <tr> <td>0805</td> <td>32</td> </tr> <tr> <td>1206</td> <td>32</td> </tr> </tbody> </table>	Style	k	0603	30	0805	32	1206	32	\pm (0.05 % R + 10 m Ω)
Style	k											
0603	30											
0805	32											
1206	32											
-	(IEC 60440) 2.5.1	Non-linearity (3 rd harmonic attenuation)	-	$A_3 \geq A_3$ min. according to diagram non-linearity								
8.3.3	2.5.2	Resistance at high and low temperature	-(55 \pm 3) °C (125 \pm 3) °C	\pm 50 ppm/K; \pm 25 ppm/K; \pm 15 ppm/K								
8.3.2	2.5.1	Resistance	(22 \pm 3) °C	\pm 1 % R; \pm 0.5 % R; \pm 0.1 % R								
8.6	-	External visual inspection	-	-								
QUALIFICATION AND PERIODIC TESTS (CHART F4)												
8.8	(IEC 60068-2-14, Na); 1.5	Rapid change of temperature	-55 °C; 30 min; 125 °C; 30 min; 10 cycles	\pm (0.1 % R + 10 m Ω)								
8.11.2		Robustness of terminations:										
8.11.2.1	(IEC 60115-1, 4.32)	Adhesion (shear test)	5 N; 10 s	No visible damage \pm (0.05 % R + 10 m Ω)								
	2.3	Bend strength of the end face plating (substrate bending test)	Depth 2 mm; 5 s; 10 times	No visible damage \pm (0.05 % R + 10 m Ω)								
8.12	(IEC 60068-2-20, Tb) 2.4	Resistance to soldering heat	Solder bath method; (260 \pm 5) °C; (10 \pm 1) s	No visible damage \pm (0.02 % R + 10 m Ω)								

TEST PROCEDURES AND REQUIREMENTS				
ESCC 4001 PARAGRAPH	ESCC 4001/029 PARAGRAPH	TEST	PROCEDURE	REQUIREMENTS PERMISSIBLE CHANGE (ΔR)
			Stability for product types:	
			TNPS0603	10.0 Ω to 221 k Ω
			TNPS0805	10.0 Ω to 422 k Ω
			TNPS1206	10.0 Ω to 1.00 M Ω
8.10	1.5	Climatic sequence:		$\pm (0.1 \% R + 20 \text{ m}\Omega)$
8.10.2	(IEC 60068-2-2, Ba)	Dry heat	125 °C; 16 h	$R_{\text{ins}} \geq 1 \text{ G}\Omega$
8.10.3	(IEC 60068-2-30, Db)	Damp heat, cyclic	55 °C; $\geq 90 \% \text{ RH}$; 24 h; 1 cycle	
8.10.4	(IEC 60068-2-1, Aa)	Cold	-55 °C; 1 h off; 0.75 h on	
8.10.5	(IEC 60068-2-13, M)	Low air pressure	2 kPa; (25 \pm 10) °C; 1 h; $U = \sqrt{P_{70}} \times R \leq U_{\text{max}}$	
8.10.6	(IEC 60068-2-30, Db)	Damp heat, cyclic	55 °C; $\geq 90 \% \text{ RH}$; 24 h; 5 cycles	
8.10.7	-	DC load	$U = \sqrt{P_{70}} \times R \leq U_{\text{max}}$; 1 min	
8.3.1.2.2	(IEC 60115-1, 4.6.1.4)	Insulation resistance	Test jig for flat chips $U = 100 \text{ V}$; 1 min	$R_{\text{ins}} \geq 1 \text{ G}\Omega$
8.3.1.3.2	(IEC 60115-1, 4.7) 1.5	Voltage proof	Test jig for flat chips $U_{\text{RMS}} = 1.4 \times U_{\text{ins RMS}}$; $f = (50 \pm 10) \text{ Hz}$; 5 s	No breakdown; no flashover
8.13	2.7 1.5	Endurance at operating life	$U = \sqrt{P_{70}} \times R \leq U_{\text{max}}$; 70 °C; 1000 h; 1.5 h on; 0.5 h off 70 °C; 1000 h 70 °C; 2000 h	$\pm (0.05 \% R + 10 \text{ m}\Omega)$ $\pm (0.1 \% R + 20 \text{ m}\Omega)$ $R_{\text{ins}} \geq 1 \text{ G}\Omega$
8.14	(IEC 60068-2-20, Ta)	Solderability	Solder bath method; SnPb40; non-activated flux (235 \pm 5) °C; (2 \pm 0.5) s	Good tinning ($\geq 95 \%$ covered); no visible damage; $\pm (0.02 \% R + 10 \text{ m}\Omega)$

DIMENSIONS



DIMENSIONS AND MASS					
TYPE / SIZE	L (mm)	W (mm)	H (mm)	T ₁ , T ₂ (mm)	MASS (mg)
TNPS0603 ESCC	1.60 \pm 0.10	0.85 \pm 0.10	0.45 \pm 0.10	0.30 \pm 0.20	≤ 2
TNPS0805 ESCC	2.00 \pm 0.15	1.25 \pm 0.15	0.45 \pm 0.10	0.40 \pm 0.20	≤ 5
TNPS1206 ESCC	3.20 \pm 0.15	1.60 \pm 0.15	0.55 \pm 0.10	0.50 \pm 0.25	≤ 10

SOLDERING RECOMMENDATIONS

For recommended solder pad dimensions please refer to www.vishay.com/doc?28950.

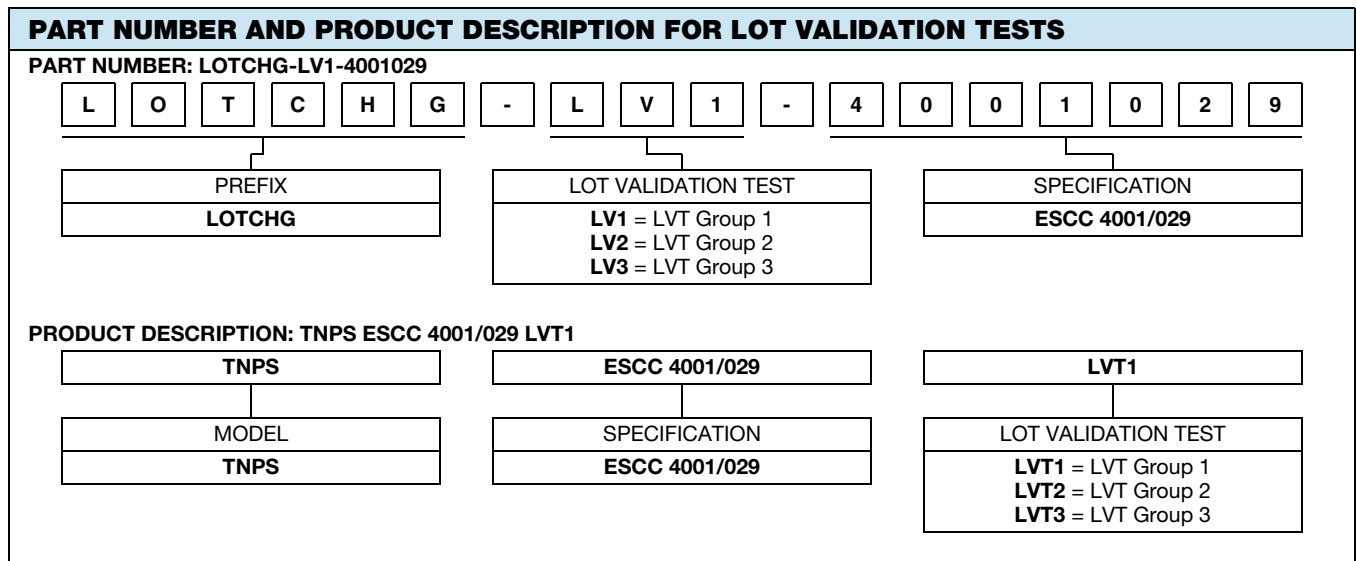
For recommended soldering profiles please refer to www.vishay.com/doc?31090.



LOT VALIDATION TESTS

Execution of Lot Validation Tests is available as a separate order item. Deliverable item to the Lot Validation Tests is the test report together with the used samples. The samples need to be ordered as a separate item.

SCOPE OF LOT VALIDATION TESTS table with columns for Group, Test Name, ESCC Reference, and Sample Count. Includes sub-groups for Environmental and Mechanical, Endurance, and Electrical and Assembly tests.



Note

- Execution of Lot Validation Tests can be ordered using either the PART NUMBER or the PRODUCT DESCRIPTION

ORDER TEXT EXAMPLE table showing a sample order line with columns for POS, QTY, ITEM, and a description of the item including part number and test group.



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