UltraSource®

Your Thin Film Source

DESIGN GUIDELINES

www.yourthinfilmsource.com

A sub-division of Vishay Intertechnology, Inc.

VISHAY ULTRASOURCE DESIGN GUIDELINES

Subhead

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Company Overview

UltraSource, Inc. was founded in 1991 with the vision to create jobs in the USA by providing thin film manufacturing services for diverse high technology customers. In 2018 UltraSource was acquired by Vishay Intertechnology to strengthen their existing thin film portfolio with our industry-leading high performance thin film circuit and interconnect capabilities. Today, we are known as Vishay UltraSource (VUSI), but we remain true to our original charter by providing our customers with the technology and quality that they need to stay competitive. Our custom 25 000 square foot facility houses a complete array of cleanrooms and equipment specially tailored for manufacturing reliable thin film products.

VUSI products are used in many applications demanding zero failures and zero downtime. Our AS9100 certification attracts and retains customers in aerospace, defense, satellite, and medical sectors where quality and high reliability are absolute musts. VUSI's high performance circuits and interconnects are integral components for electronic and optical equipment designed and manufactured to provide a lifetime of reliable performance. Our quality performance proves to our customers that VUSI is committed to producing quality products that meet all customer expectations.

Our customers expect 100 % on-time delivery performance, which is no easy task when building the complex custom products that we manufacture. In response to customer expectations, we have developed a comprehensive scheduling and planning software system that enables us to manage supply and demand. Complex manufacturing routings are programmed with set-up and run times and the software system schedules the work centers in the factory. Extensive analysis and management of daily execution keeps orders running and shipping on time.

Our customers are located all over the world, but manufacturing and fabrication is performed in our facility located in southern New Hampshire.

Sales Quote

Please send all requests for quotes to your account manager or the following e-mail address: UltraSource@Vishay.com. The following information should be included in the RFQ:

- Quantities and lead times to quote
- CAD data package (in AutoCAD DWG or DXF format)
- Detailed fabrication drawing
- Referenced standards or specifications (latest revision is critical!)
- Quotation due date

Upon receipt, VUSI enters your request into our quoting system and prioritizes a response per your requirements. Our standard quote turnaround is within 24 hours, but most RFQs can be completed in less than two hours if requested (complex products or a large number of part numbers may require more analysis).

Every quotation package we receive is custom-quoted (provided the required information is available and complete) in order to compute an accurate price and delivery quotation. Any assumptions made at the time of the quote are clearly listed on our quote form, and will need to be resolved / confirmed prior to order acceptance during contract review.

VUSI's quotes are typically valid for 30 days after generation, and we meticulously file all quotes, CAD data, and drawings (which will be used to produce the part when the order is received). Any changes to the CAD data package, fabrication requirements, array configuration, or deliverable requirements will likely require us to revise our quotation in order to ensure price and lead time accuracy.

CAD Quality and Workmanship

How Your CAD File Affects the Success of Your New Thin Film Design

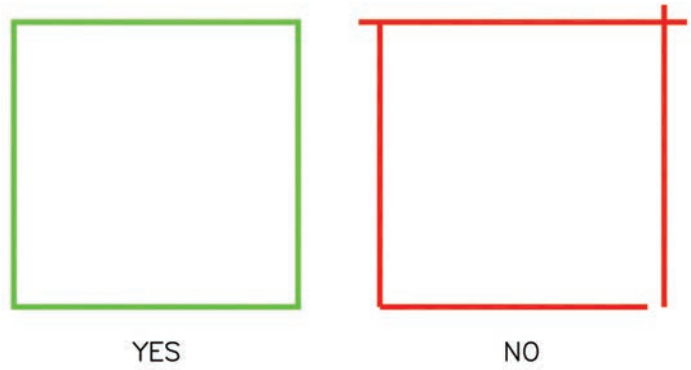
At VUSI, customer-supplied CAD files play a critical role in supporting the manufacture of every thin film component we build. Customer-furnished CAD files are used to fabricate the photomasks that are used in manufacturing to pattern the circuit images via photolithography and etching on to the ceramic substrate. And although our customers typically know that the preparation of the photomasks is a critical part of the thin film manufacturing processes, we find that CAD files will often contain layout and / or data errors.

Today's complex thin film components increasingly require more physical layers and features. A few years ago the typical thin film component may only have required two or three layers. Now, common designs require up to six layers and sophisticated designs need up to twelve layers. A modern thin film component or circuit design may include many elements, such as tuning pads, RF or microwave features, optical features, resistors, capacitors, vias, selective solder pads, solder stops, polyimide dielectrics, vision recognition alignment targets, and custom serialization. If the CAD design contains data or layout errors such as gaps and misalignments in between the polygons that make up the design, detecting and repairing the errors may cause a significant delay in the fabrication of the photomask(s) and the end products. In a worst-case scenario, data or layout errors in the CAD can cause an erroneous design to be fabricated.

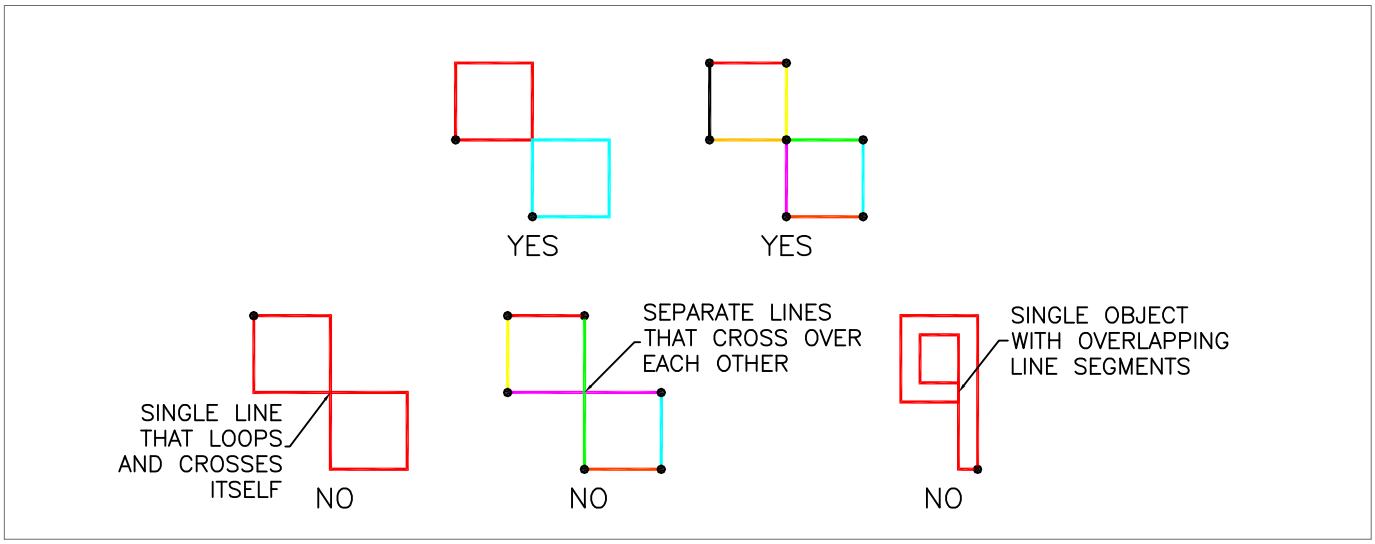
The key to reducing the time to market and avoiding errors is for customers designing thin film components and circuits to be diligent in generating CAD designs that follow industry standards and generally accepted good practices. By keeping these design rules in mind, you can avoid the order delays resulting from most CAD issues. We derived these 10 rules from the most common issues we encounter in our daily design and CAD review processes.

Please Read Carefully and Integrate These Rules into Future CAD Designs in Order to Avoid Processing Delays

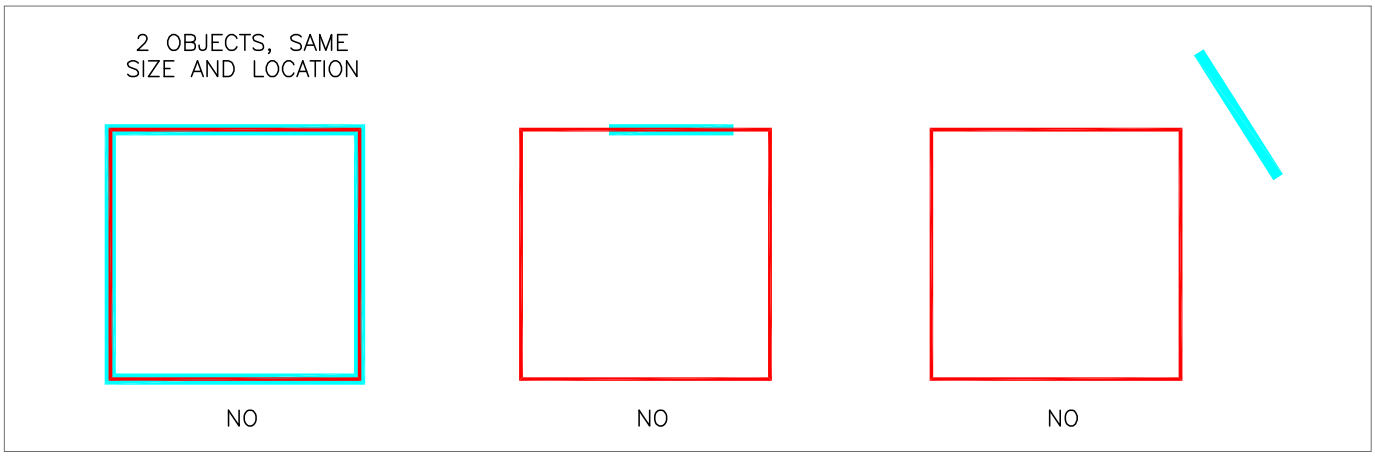
1. The preferred file format is AutoCAD DWG or DXF. VUSI does not prefer Gerber or GDS files, as hard to detect translation errors may occur during the conversion to the AutoCAD format
2. Files must be two-dimensional with the units and scale clearly specified
3. Zero-width polylines should be used to create closed boundary polylines for all patterned geometries



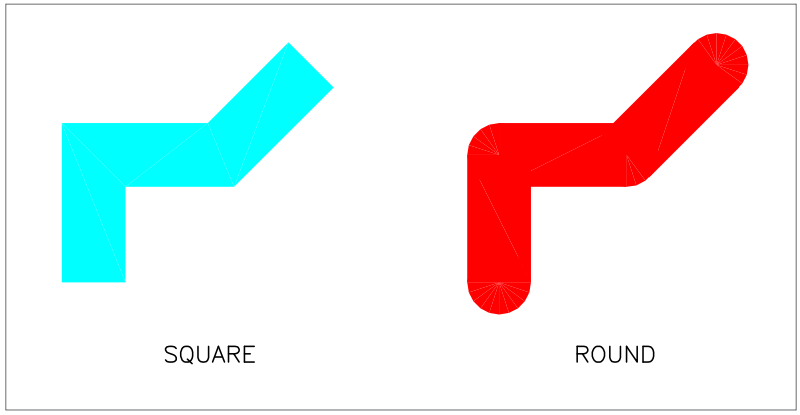
4. Polylines must not result in self-intersecting boundaries. The bold dots in the image below indicate the start and stop points for line segments



5. Avoid double entities or extraneous lines



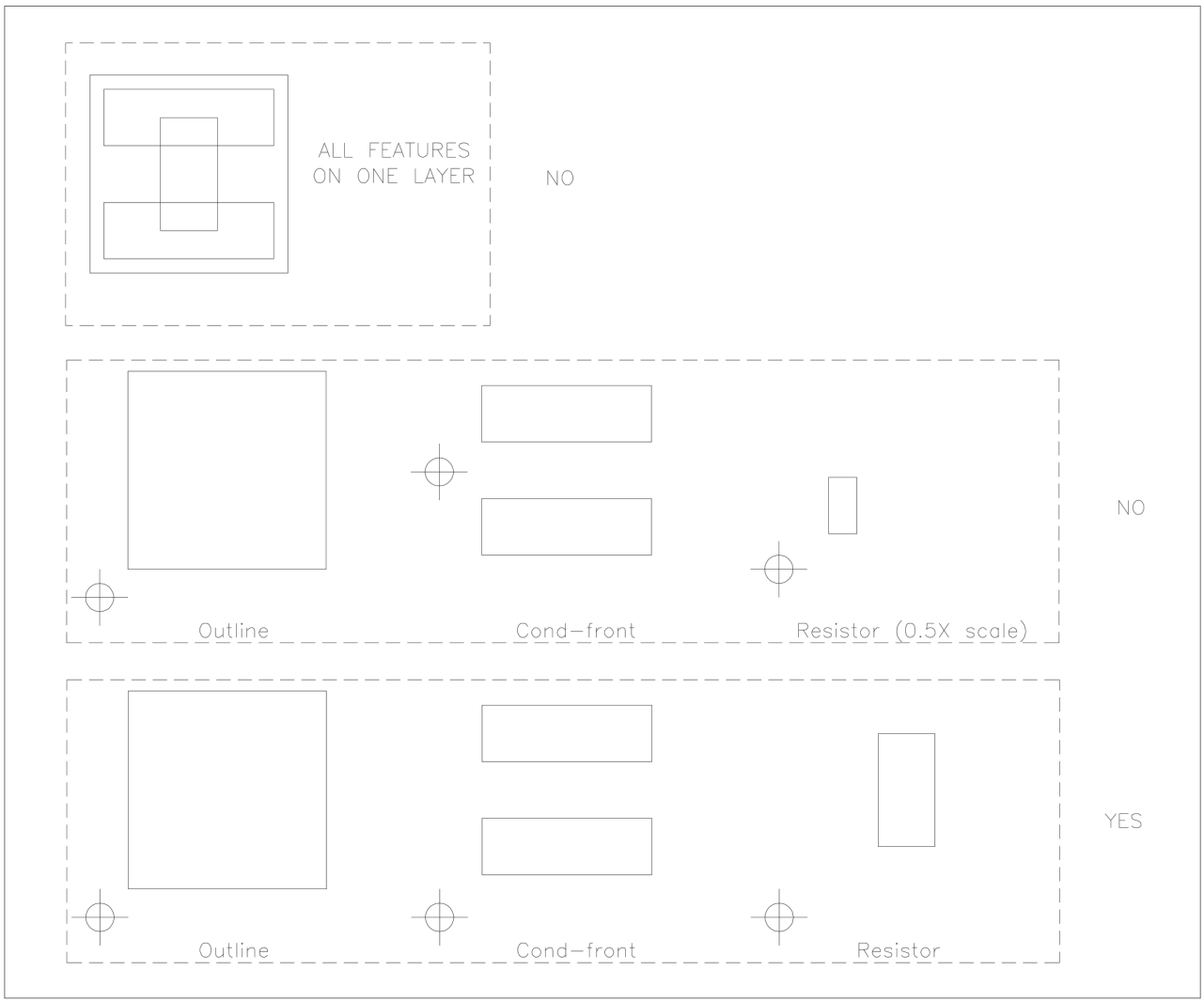
6. If polylines with a width are used, the corner type must be stated. The default method varies between the various design software packages, and the AutoCAD standard is a square corner



7. Each different metal or mechanical pattern should be drawn on a separate layer, preferably with descriptive layer names as shown in the table:

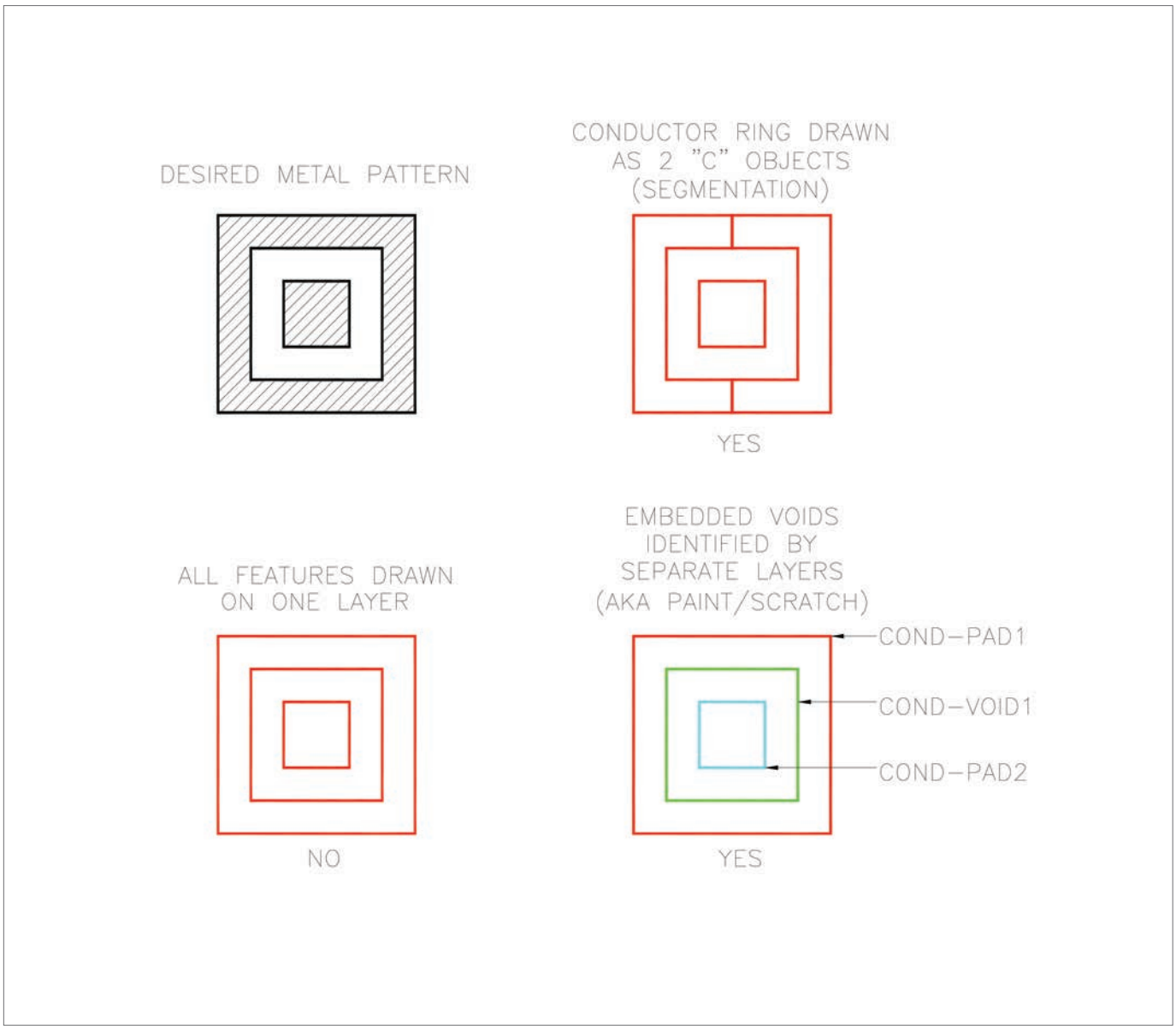
Sample Layer Name	Description
Outline	Mechanical outline of circuit
Cond-front	Conductor layer, specifying front or back side
Notes	Non-pattern features, including notes or dimensions
Resistor	Resistor layer
Via	Metallized through hole
AuSn	Pre-deposited solder layer

8. If the design software does not allow the exporting of a file with more than one layer, then each metal or mechanical pattern should be exported separately using the identical scale and origin



9. Patterned circuit text should be drawn using zero-width polylines. If typed text must be used, limit the font type to either RomanS or TXT

10. Voids within patterned features must be clearly identified. Acceptable methods include the use of segmentation or layer names to identify voided objects



Fabrication Drawing Importance

In order for the quotation to be accurate and to ensure that the build process goes smoothly and efficiently, customer-supplied design specifications should be as clear as possible. Because of the complexity of thin film designs, drawings should be revision-controlled and complete so that a large amount of time is not spent clarifying the actual requirements before we can issue a quotation and can start to build the job.

Revision-controlled fabrication drawings create clarity and accountability for all parties and the lack of an accurate fabrication drawing threatens the quality and design accuracy. This is especially true as designs get more complex.

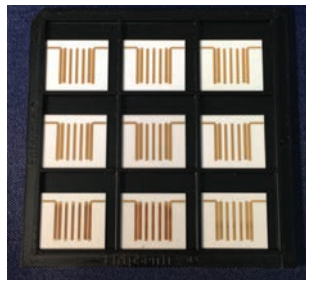
It is important for our customers to realize that seemingly minor assumptions during manufacturing can affect the ultimate quality or performance of thin film circuit design. Quality or performance issues create unnecessary competitive or profit risk for both VUSI and our customers. Therefore, revision-controlled fabrication drawings are important to both parties.

Fabrication drawings provide many important functions in support of the thin film manufacturing process:

- Fabrication drawings provide all the important information about the design that is needed to prepare a quote
- Fabrication drawings should ideally add the extra details about the design that aren't easily incorporated into the CAD files, such as material and tolerances
- A good fabrication drawing will include the criteria by which the finished product will be evaluated for acceptability
- Fabrication drawings serve as a tool to be used during final inspection
- A fabrication drawing is a revision-controlled record that stores the details of a product by title, part number, and revision
- The notes on a fabrication drawing are like an instruction manual for building your product just like you want or need it

Substrate Materials

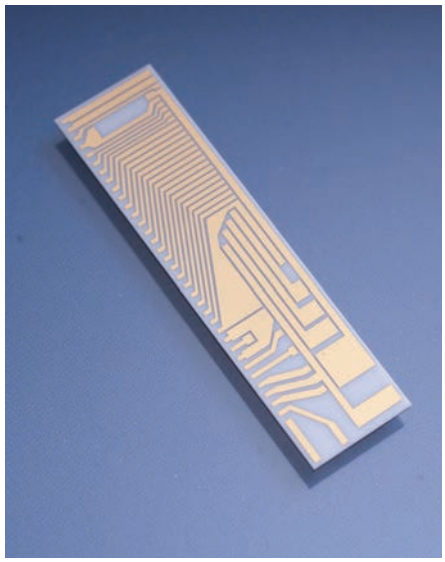
The substrate is the foundation on which thin film components are built. The substrate properties have significant influence on the performance of the device. Alumina is still the most common substrate material due to its surface quality, cost, and high frequency performance. For power applications the high thermal conductivity of aluminum nitride and BeO substrates makes them the best choice. Fused silica and quartz are used at very high operating frequencies. Sapphire gets called on for optical window use or when high mechanical strength is a must.



Material	Dielectric Constant (εr)	Loss Tangent (ε)	Thermal Conductivity (W/mK)	CTE (ppm/K)	Dielectric Strength (kV/mm)	Polished Surface Finish (μ")	As-Fired Surface Finish (μ")	Lapped Surface Finish (μ")	Available Thicknesses (in/mm)
99.6 % alumina	9.9	0.0001	27	7.0	23	< 1	< 4	< 10	0.005 – 0.050 (0.127 – 1.27)
99.5 % alumina	9.8	0.0001	25	7.0	23	< 2	< 5	< 20	0.005 – 0.050 (0.127 – 1.27)
96 % alumina	9.6	0.0002	25	8.2	19	< 4	< 35	< 35	0.010 – 0.120 (0.254 – 3.05)
Aluminum nitride (AlN)	8.9	0.001	170, 200, 230	4.5	15	< 4	N/A	< 20	0.005 – 0.050 (0.127 – 1.27)
99.5 % BeO	6.6	0.003	285 or 325	7.5	14	< 4	N/A	< 30	0.005 – 0.050 (0.127 – 1.27)
Fused silica	3.8	0.0001	1.38	0.5	100	60 / 40	N/A	< 10	0.005 – 0.050 (0.127 – 1.27)
Sapphire	10	0.0001	42	5	48	60 / 40	N/A	< 10	0.005 – 0.050 (0.127 – 1.27)
Borosilicate glass	5	0.003	3.2	1.2	38	60 / 40	N/A	< 10	0.005 – 0.050 (0.127 – 1.27)
Ferrites	Hundreds of ferrite formulations to choose from					< 5	N/A	< 30	0.010 – 0.050 (0.254 – 1.27)

*The material properties presented in this design guide are provided by Vishay UltraSource, Inc. (VUSI) as a service to its customers for informational purposes only. VUSI assumes no responsibility for any errors or omissions in these materials. VUSI makes no commitment to update the information contained herein.

Metalization Schemes



The metalization selection for a thin film design is critical to the success of that product. The metalization scheme is defined as the metal layers that make up the lines and features on a thin film circuit or interconnect. A typical metalization scheme consists of an adhesive layer, a solder layer, and a conductor layer. If a design includes integrated resistors, then the adhesive layer serves double duty as a controlled resistive layer and the adhesive layer.

The metalization scheme plays a huge role in electrical or optical device performance, providing component and die to substrate connections, and substrate to package connections. The metalization scheme needs to meet a long list of performance requirements, depending on the application:

- Electrical conductivity
- Thermal conductivity
- Solderability
- Wire bondability
- Epoxy adhesion
- Reliability (tape test, shock, vibration, thermal, die shear)
- Corrosion resistance
- Optical flatness
- Compatibility with lead (Pb)-free SAC-type solder alloys for RoHS compliance
- Power handling
- Cost
- Minimum line and space resolution
- Reworkable during assembly (multiple cycles)
- Maximum service temperature (high and low)
- Ability to integrate with holes, filled vias, resistors, capacitors, solder dams, crossovers, etc.

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Thin Film Design Basics Subhead

The elimination of lead from electronic devices as mandated by the Restriction of Hazardous Substances (RoHS) is changing the playing field for many global manufacturers. This is driving a transition among many customers from nickel to palladium as a SAC-compatible solder layer (SAC = SnAgCu or tin / silver / copper). SAC alloys have become the prevailing solder alloy to replace tin-lead solders. Palladium (1 $x10^7$ S/m) is slightly less electrically conductive than nickel (1.4 x 10^7 S/m) but it is still well suited for high frequency applications. Palladium also causes fewer solder problems (from Ni-Au diffusion) than nickel.

There isn't one single metalization that is a "one size fits all." A metalization scheme must be custom designed and optimized based on your specific product application. At VUSI, we can offer you many different metalization schemes for your next design, depending on whether you need low cost or high reliability, Pb / Sn or lead (Pb)-free solderability, or low power or high power. We can supply low cost, high volume products and we can also supply hi-rel Class K products. We stand by ready to assist you in making a wise choice for the metalization scheme on your next thin film design and to manufacture your devices.

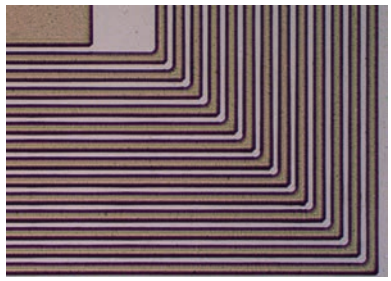
A summary of the common thin film metalization schemes is listed in the following table:

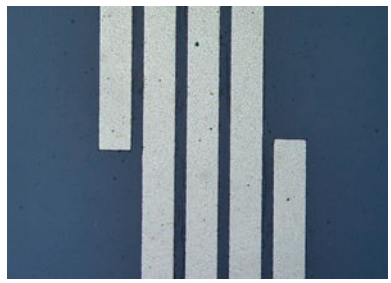
Typical Metalization	Application(s)	Comments	Attachment Method(s)	Thicknesses	Typical Value
TiW / Au	Devices requiring assembly at higher temperatures (up to 450 °C)	Barrier layer recommended for eutectic attach	Epoxies: Au / Ge, Pb / In, Au / Sn eutectic; Wire bonding	TiW 400 Å – 600 Å Au 80 µin – 240 µin	500 Å 120 µin
TiW / Ni / Au	Devices requiring solder compatibility. Watch for gold embrittlement or Ni diffusion	Maximum compatible temperature is 300 °C	Epoxies: Pb / In, Pb / Sn, Au / Sn eutectic; Wire bonding	TiW 400 Å – 600 Å Ni 4 µin – 40 µin Au 20 µin – 240 µin	500 Å 8 µin 80 µin
TiW / Pd / Au	Devices requiring solder compatibility. Keep gold thin to avoid embrittlement	Maximum compatible temperature is 300 °C	Epoxies: Pb / In, Au / Sn eutectic; Wire bonding	TiW 400 Å – 600 Å Pd 4 µin – 40 µin Au 20 µin – 240 µin	500 Å 8 µin 80 µin
TaN / TiW / Au	Resistor film requiring assembly at higher temperatures (up to 450 °C)	Not Pb / Sn solderable	Epoxies: Au / Ge, Pb / In, Au / Sn eutectic; Wire bonding	TaN 20 Ω/□ – 100 Ω/□ TiW 400 Å – 600 Å Au 80 µin – 240 µin	50 Ω/□ 500 Å 120 µin
TaN / TiW / Ni / Au	Resistor film requiring solder compatibility. Watch for gold embrittlement or Ni diffusion	Maximum compatible temperature is 300 °C	Epoxies: Pb / Sn, Pb / In, Au / Sn eutectic; Wire bonding	TaN 20 Ω/□– 100 Ω/□ TiW 400 Å – 600 Å Ni 4 µin – 40 µin Au 80 µin – 240 µin	50 Ω/□ 500 Å 8 µin 80 µin

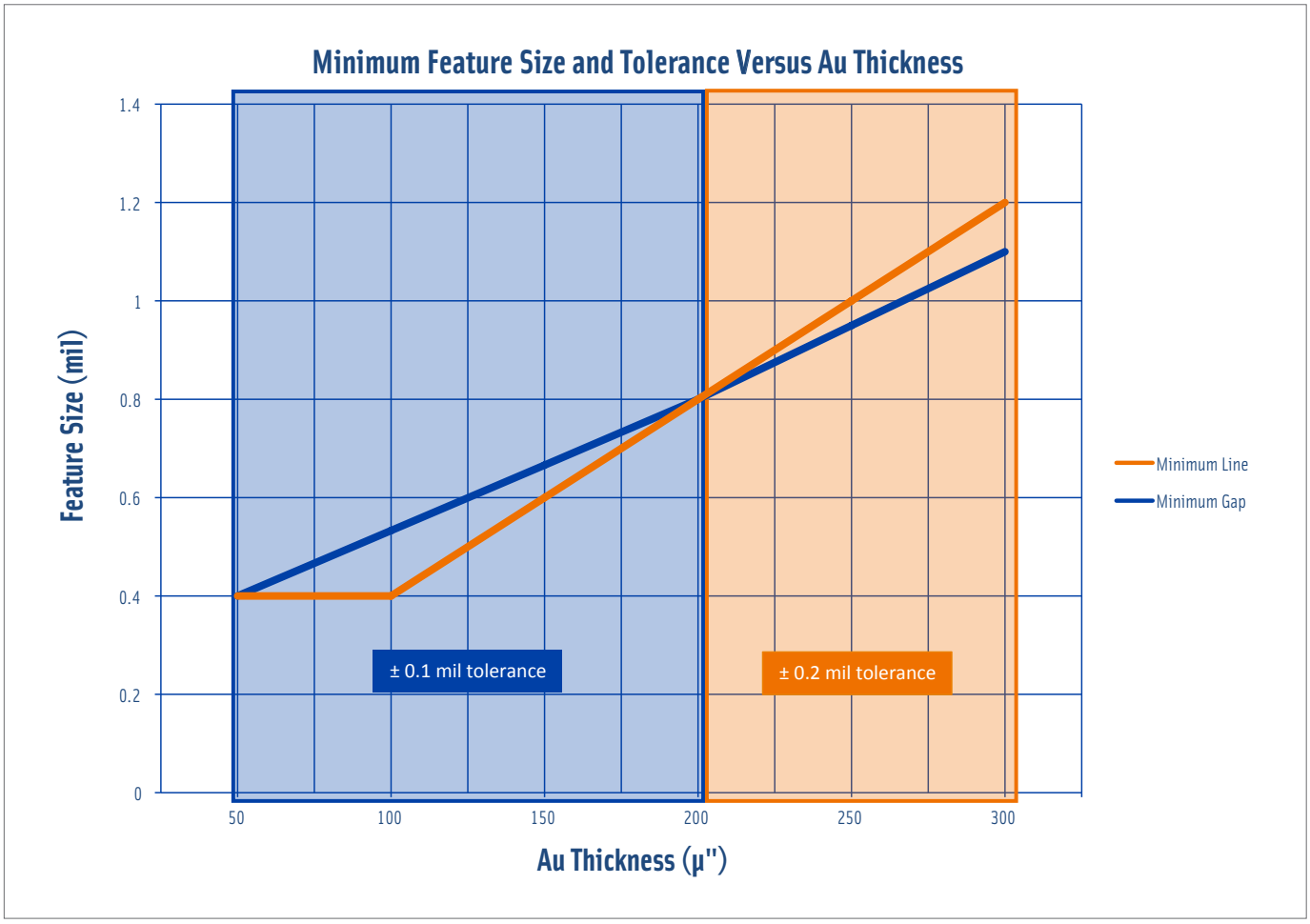
Pattern and Etch Features & Tolerances

The quality and precision of circuit patterns are two of the many advantages available when using thin film technology. Highly capable photolithography and patterning performed under comprehensive process controls provide robust pattern consistency at production volumes. Extremely small features and tolerances are available to enable high frequency design elements and performance. This also places importance on the quality and workmanship of the CAD data.

In general, if features are properly resolved in CAD and they are large enough in size, they can then be reproduced on a thin film circuit pattern. However, conductor metal thickness plays a role on pattern tolerance and minimum geometry. Essentially, the thinner the conductor metal thickness, the smaller the pattern tolerance and minimum capable geometry. The relationships between conductor metal thickness, pattern tolerance, and minimum geometry are shown in the following graph:





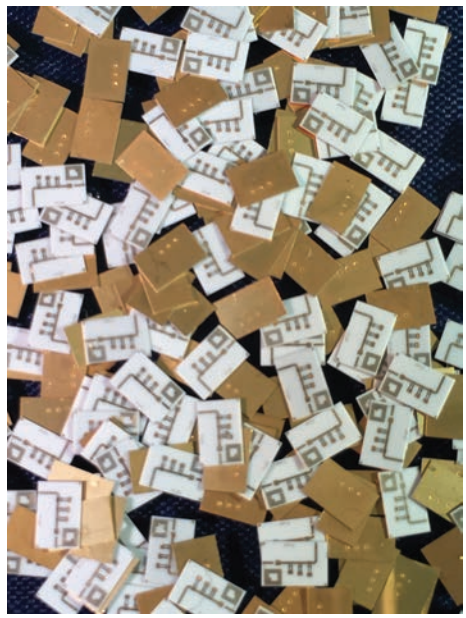


Mechanical Guidelines (Dicing or Laser Machining)

Since most thin film devices are designed on hard, ceramic materials, the majority of devices are machined to size by using a high speed diamond cutting blade, or dicing. However, dicing is limited to only making straight line cuts. When a thin film device needs holes, cut-outs, chamfers, radii, or perimeter contouring, CO_2 laser machining is employed, often in tandem with dicing. The design focus for dicing and laser machining needs to be concerned with mechanical machining tolerances and keeping metal away from the areas to be machined (this is called metal pull-back). Listed below are the mechanical guidelines for dicing and laser machining:

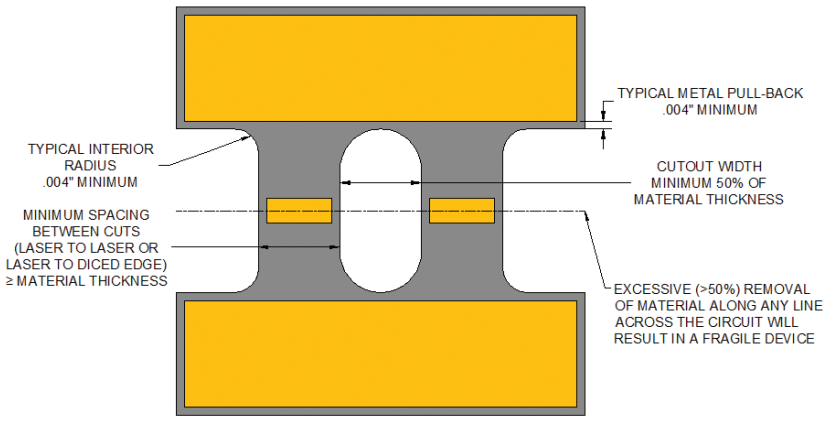
Dicing	Comments
Substrate types	All substrate materials
Metal pull-back from circuit edge*	0.002 in (50 µm) min. Both front and back
Dicing tolerance	± 0.002 in (50 µm) standard ± 0.001 in (25 µm) special

* Without a properly designed metal pull-back there will be a burr raised on the edges of the devices by the dicing blade.



Laser Machining	Comments
Substrate types	All substrate materials
Metal pull-back from circuit edge*	0.004 in minimum (100 µm) Both front and back
Machining tolerance	± 0.002 in (50 µm)

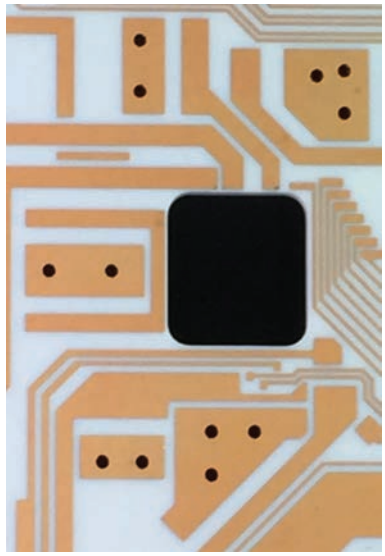
* Without a properly designed metal pull-back there will be a burr raised near all laser cuts by the laser beam.



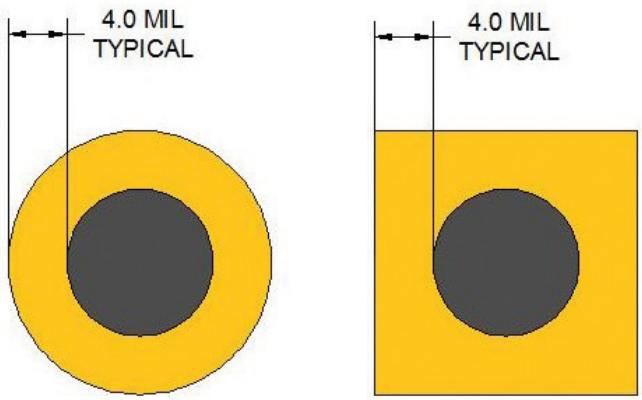
Plated Through Holes and Slots

VUSI offers plated through holes (vias) and slots in most of the substrate materials that we process. Plated through holes and slots provide reliable electrical paths to the ground plane or backside pattern. These connections provide a convenient, compact means of obtaining a ground connection without needing to use ribbon bonds or conductive epoxy. Most of the time the metalization is fully sputtered in order to provide optimal adhesion and reliability, but the metalization can also be electroplated, depending on the designated metalization scheme.

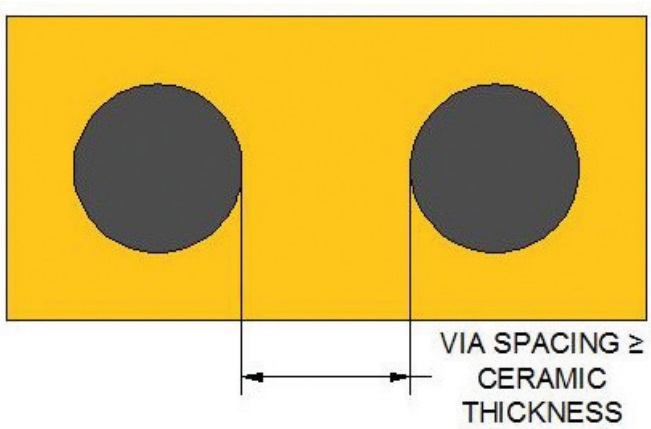
The plated through holes and slots are laser machined into the substrates and then specially cleaned in order to remove any laser slag. There are a few design concerns with plated through holes and slots; namely, maintaining a proper aspect ratio (ratio of the hole diameter to the substrate thickness) so the hole barrels fully metalize and maintaining large enough capture pads (annular ring or border).



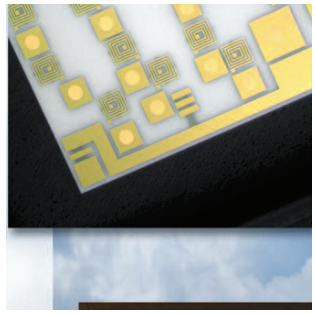
Design Guidelines	Plated Through Holes
Capture pad	See picture to right
Hole to hole spacing	See picture to right
Via location tolerance	± 0.002 in (50 µm)
Via diameter tolerance	± 0.002 in (50 µm)



Substrate Thickness (in)	Allowable Hole Diameter Ranges (in)
0.005	0.003 – 0.005
0.010	0.006 – 0.010
0.015	0.008 – 0.015
0.020	0.010 – 0.018
0.025	0.012 – 0.020



Filled Vias (Gold and Copper)

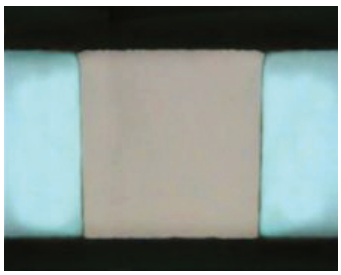


VUSI has developed gold- and copper-filled via products to provide robust, highly conductive, reliable connections through thin film substrates. Our pure gold- and copper-filled vias set the standard for high performance filled via technology by eliminating epoxy or solder bleed-through while enhancing via conductivity and reliability. The pure gold-filled via is called the UltraVia and the pure copper product is called the CopperVia. The UltraVia is a hi-rel product that has been qualified by many customers for use in space, cryogenic, and defense applications.

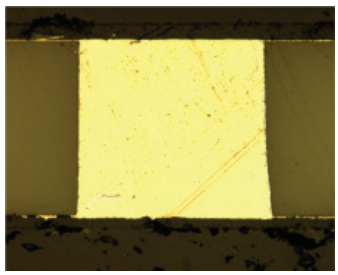
VUSI filled vias are used to:

- Eliminate the epoxy or solder extrusion and bleed-through that can occur during die and housing assembly when using plated through holes or thick film filled vias
- Create efficient heatsinking when high power devices are mounted on top of the thin film substrate
- Create low inductance or low resistance ground connections through the thin film substrate

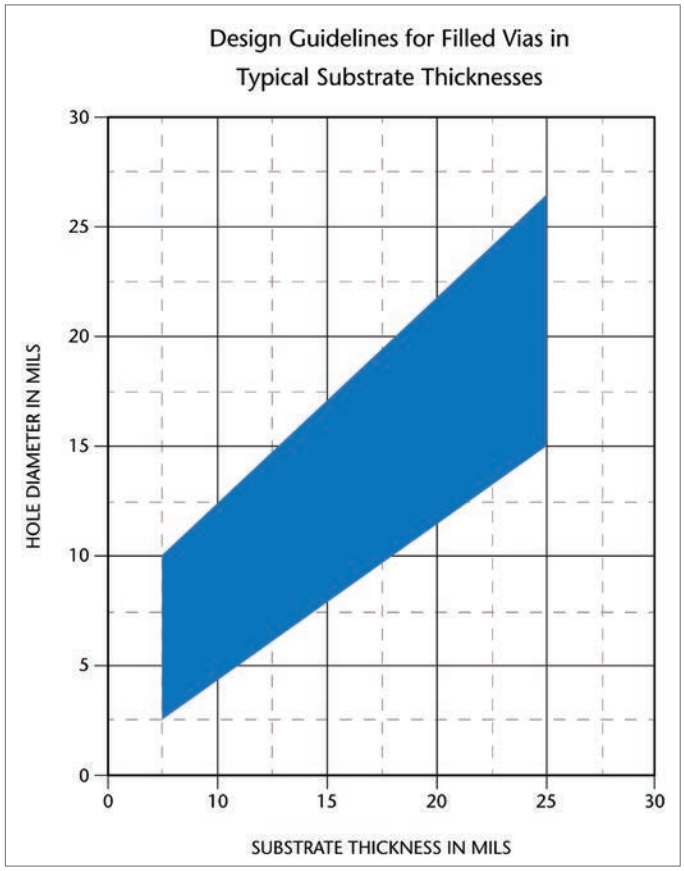
Design Guidelines	UltraVia	CopperVia
Fill material	Pure gold	Pure copper
Thermal conductivity	318 W/mK	400 W/mK
Space qualified	Yes	No
Substrate materials	Alumina, AlN, BeO	
Via location tolerance	± 0.002 in (50 µm)	
Via diameter tolerance	± 0.002 in (50 µm)	
Via planarity	± 0.0002 in (5 µm)	
Minimum capture pad	Via diameter + 0.004 in (100 µm)	



CopperVia Cross Section



Pure Gold UltraVia Cross Section



Resistor Design

A basic understanding of thin film resistor designs is required if you want to integrate sheet resistors in your circuit. Thin film sheet resistors are typically fabricated by sputtering a film of tantalum nitride (TaN) under the conductor layer and then selectively etching the resistor elements. TaN resistors are very stable and reliable after they are passivated at high temperatures. Nichrome (NiCr) resistors are used in specialty applications where a low temperature coefficient of resistance (TCR) is required.

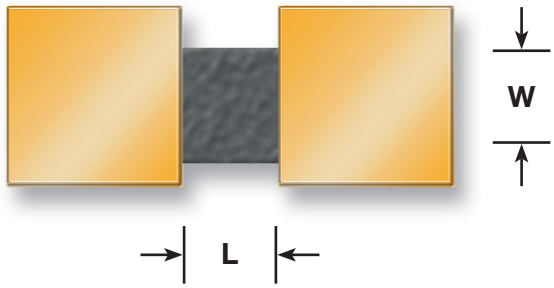
Resistor Film	Available Sheet Resistivity	Self-Passivating	TCR (ppm/°C)	Stability*
TaN	25 Ω/□ - 200 Ω/□	Yes	-125 ± 50	< 0.5 %
NiCr	40 Ω/□ - 240 Ω/□	No	0 ± 50	< 0.5 %

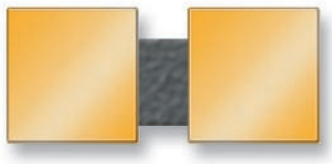
*ΔR/R after 1 000 hour bake at 125 °C

Once you have selected a resistor film type and desired resistivity, the elements are designed under the following rules:

R = ρ L / W, where R = total resistance of the element (Ω), **ρ** = sheet resistivity (Ω/□), **L** = resistor length (distance between the conductors), and **W** = resistor width (width of the resistor element).

This formula demonstrates that the aspect ratio of L/W becomes a simple means of designing for the total resistance of the element. Examples of resistor elements, using a 50 Ω/□ film, are demonstrated here:





L = 0.5 W
L / W = 0.5
R = 25 Ω

L = 1.0 W
L / W = 1.0
R = 50 Ω

L = 2.0 W
L / W = 2.0
R = 100 Ω

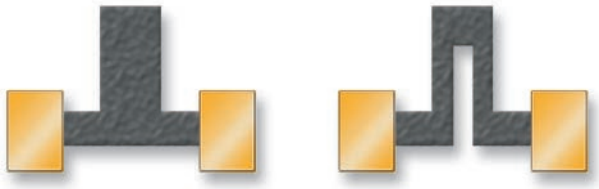
Laser Trimming vs. Passivate Only

Block elements, meander resistors, and top hat elements are the three primary types of thin film resistor layouts. Laser trimming uses a YAG laser system to measure individual resistors and uptrims the resistor values to tighter tolerances. Uptrimming works by reducing the width of resistor elements through laser ablation. Laser trimming can be used to obtain tolerances as small as ± 25 %, but standard laser trim tolerances are ± 1 %, 2 %, 5 %, and 10 %. Modern laser trim equipment is fast and economical for most applications.

Block elements are used as a low value resistor element:

Meander resistors are used as a high value resistor element, but placed in series with a top hat element that provides a reliable laser trim. **Note:** when calculating the L / W of the total element, each right angle turn adds 0.5 squares to the total.

Top hat elements are used as a high value laser-trimmable resistor element:



Design considerations for laser-trimmed vs. passivate only:

Some customers reduce fabrication costs by opening up the allowable resistor tolerances to ± 10 % or 20 %, so that laser trimming can be avoided. This is called passivate only and has different layout considerations than laser trimming:

a) Resistors that will be passivated then laser trimmed should be designed at 80 % of nominal value in the CAD data. This requirement ensures that none of the resistors will passivate “over-value” prior to trimming.

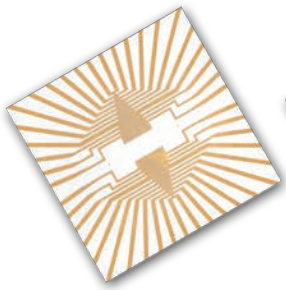
b) Resistors that will be passivated only (not trimmed) should be designed at nominal value in the CAD data, or 100 % of final intended value.

Critical Note	Laser Trimming	Passivate Only
Layout resistors at:	80 % of final (R) value	100 % of final (R) value

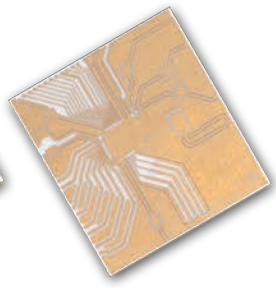
UltraFAST Rapid Prototyping Service

This is the new economy where all customers want their products faster than ever. Enter UltraFAST, the first and only thin film prototyping program of its kind. Rather than waiting weeks for your critical prototypes, VUSI can build them in a matter of days so you can rapidly produce and test your new designs.

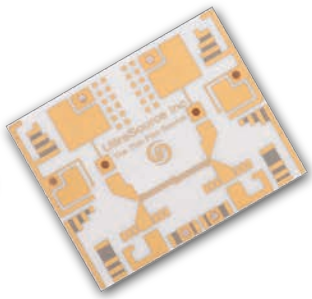
In 2010 we invented the UltraFAST program so we could meet the challenge of delivering product in days. The program uses a dedicated team of people employed in a streamlined manufacturing approach to build rapid prototypes. Take advantage of the expertise of the UltraFAST team and you'll be getting your prototypes faster than ever before. UltraFAST is designed to offer a comprehensive range of standard single-sided and double-sided designs compatible with a broad range of traditional thin film circuit requirements. The substrate choices, metalization systems, and integration options have been selected to allow you to further increase device function and performance while reducing prototyping costs.



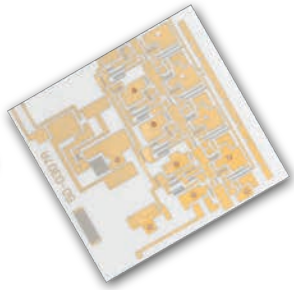
1 - Sided Conductor
4 Days



2 - Sided Conductor
5 Days



1 - Sided Conductor
with Resistors
6 Days



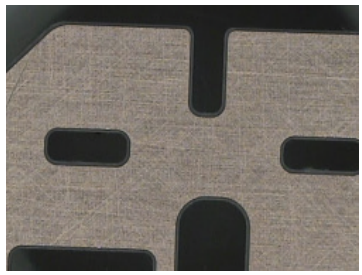
2 - Sided Conductor
with Resistors
7 Days

We realize that the standard options available through the UltraFAST program will not meet the requirements for every customer, so we've built custom flexibility into the program. If you need a metal, material, or features that are not listed in the UltraFAST standard options, please contact our sales department to request a custom rapid prototype program for you.

The UltraFAST program details are maintained on the VUSI company website. Please go to **www.yourthinfilmsource.com** for up to date details on the program.

UltraFAST Option	Lead Time in Working Days
1-Sided Conductor (metal on one side)	4
2-Sided Conductor (metal on two sides)	5
1-Sided Conductor and Resistor	6
2-Sided Conductor and Resistor	7
Pizza Mask (multiple P / N on one substrate)	+1
CopperVia*	+14 or 0*
Plated Through Holes	+5
Post Laser Machining	+2
*Order your CopperVia pattern as soon as the hole location design is fixed so the substrates are ready at the start of your UltraFAST order.	

Backside Burnishing for Epoxy Adhesion Enhancement



When bonding thin film components to carriers and housings with epoxy, the success of the application depends not only on the strength of the epoxy, but also on how well the epoxy adheres to the surface to which it is being applied. In most cases, the strength of the bond relies on the epoxy's ability to mechanically "key" into clean, dry, mating surfaces.

That is why the following three steps of surface preparation are critical to successful epoxy bonding:

- **Clean** — Mating surfaces must be free of any contaminants such as grease, oil, fingerprints, or mold release. Contaminated surfaces should be cleaned with solvents or plasma cleaning to ensure an atomically clean surface. Plasma cleaning should ideally be performed immediately before epoxy bonding. Follow all safety precautions when working with solvents
- **Dry** — All surfaces to be bonded must be as dry as possible for good adhesion. If necessary, accelerate drying by using filtered air, nitrogen gun, or short oven bake.
- **Burnishing** — When high reliability bonding is desired, it is ideal to "burnish" the mating surfaces so the epoxy has a mechanical pattern for the epoxy to "key" into. Backside burnishing is a unique backside metalization treatment developed at VUSI to enhance the adherence of thin film components to carriers by epoxies.

Backside burnishing results in a backside metalization surface that has greatly improved adhesion over standard metalization schemes. This surface modification technique provides a cross-hatched 4 µin to 8 µin surface finish that allows the epoxy to attach itself securely and key into the texture of the surface, therefore reducing delaminating and peeling issues. This method of attachment has proven to be effective with substrates attached to carriers or metal housings. Backside burnishing treatment is carefully controlled so it textures the gold surface but does not reduce the gold thickness, so electrical performance is unaffected. This surface treatment will often result in improved adhesion and eliminate the need for customers to roughen up the surface of the components themselves before epoxy bonding.

Many of our customers have tested and qualified this backside surface treatment for commercial, defense, and satellite use.

To add backside burnishing to your design, simply add a note specifying backside burnishing as a requirement to your fabrication drawing.

Gold-Tin Deposited and Patterned Solder

Selectively deposited gold-tin (Au / Sn) solder has become an important tool in the effort to reduce the size of thin film electronic and optoelectronic modules. Selectively deposited and patterned Au / Sn solder enables lower cost assembly processes and higher assembly yields by precisely placing high quality solder exactly where it is needed. This avoids the expense and issues with buying, stocking, and placing solder preforms. There are usually substantial cost savings by using Au / Sn deposited and patterned solder when a design requires a high number of solder locations and sub-mounts or circuits are being assembled in production quantities.

Vacuum-deposited Au / Sn solder composition can be deposited in compositions of 80 / 20 to 73 / 27. VUSI can deposit thin layers of Au / Sn solder in custom thicknesses from 2 µm to 8 µm with a thickness tolerance of ± 20 %.

Au / Sn Guidelines	Values
Smallest feature size	0.004 in x 0.004 in (100 µm x 100 µm)
Typical Au / Sn film thickness	160 µin - 240 µin (4 µm - 6 µm)
Minimum Au / Sn film thickness	80 µin (2 µm)
Maximum Au / Sn thickness	320 µin (8 µm)
Minimum space between Au / Sn pads	0.002 in (50 µm)
Tolerance on thickness of Au / Sn films	± 20 %
Placement accuracy of Au / Sn patterns	± 0.0005 in (± 12.5 µm)
Minimum pull-back from laser cut edge	± 0.002 in (± 50 µm)

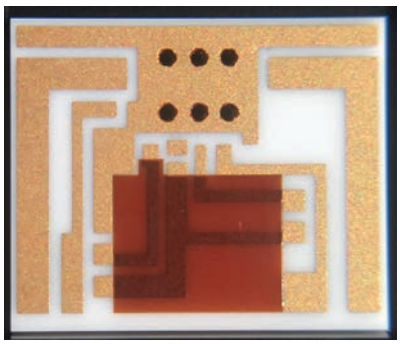
Polyimide

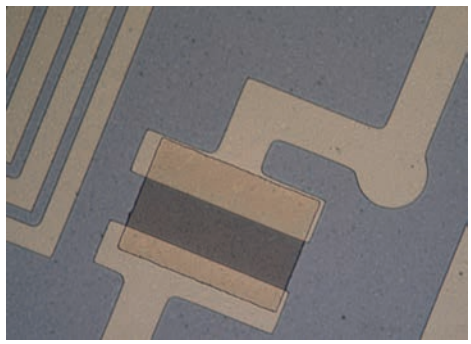
Polyimide is a polymer material known for its thermal stability, good chemical resistance, and excellent mechanical properties. The cured film properties of polyimide allow it to be used as a dielectric feature in thin film applications in order to provide performance or assembly benefits. Polyimide coatings are being used more and more as customized, integrated 3D dielectric coatings on thin film circuits and interconnects. There are now four common uses of polyimide coatings that thin film circuit designers should be aware of:

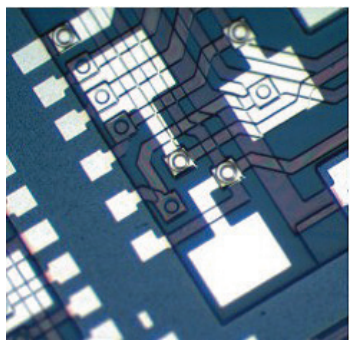
1. **Solder Dams** – A polyimide solder dam is a strip of material placed strategically across lines or pads to stop the flow of solder from one location to another
2. **Crossovers** – In Lange couplers and similar devices where there is a need to replace wire bonds with a robust crossover, crossovers supported by cured polyimide provide a rugged, highly reliable structure
3. **Mechanical Protection Layer** – Polyimide is very useful as a mechanical protection layer. It is used to protect fine pitch or critical circuit areas from assembly damage
4. **Multilayer** – Polyimide offers the ability to build up multiple layers of circuitry and dielectric on thin film circuits on ceramic, thus providing the ultimate option for reducing size and increasing signal speed

The properties of polyimide are presented in the following table:

Property	Value
Tensile strength	200 MPa
Elongation	45 %
Young's modulus	3.5 GPa
Water absorption	1.3 %
Tg value (TMA)	325 °C
CTE	35 ppm
Dielectric constant	3.3
Dissipation factor	0.001
Dielectric strength	250 kV/mm
Volume resistivity	2.5×10^{16} Ω/cm

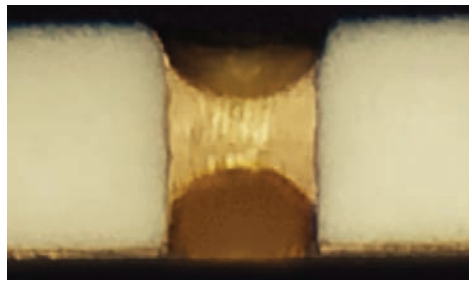






PolyVia

The PolyVia product is a epoxy-based plugged via option that customers can add to their plated through-hole designs in order to stop epoxy or solder bleed-through during assembly operations. The technology uses a epoxy resin that is deposited into each plated through hole and then cured. Once cured, the PolyVia plugs exhibit excellent adhesion and thermal stability to gold and other thin film metal films. The PolyVia system eliminates epoxy or solder bleed-through, but at a lower cost than the pure metal-filled via products like the UltraVia or CopperVia that VUSI offers.



The PolyVia has many performance benefits:

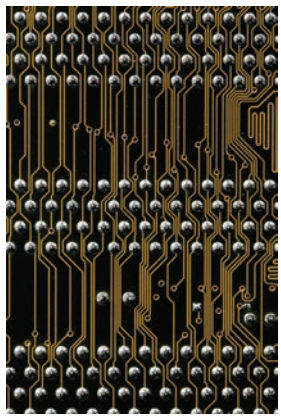
- Eliminates the mess and rework associated with epoxy or solder bleed-through, which can occur during die and housing assembly from plated through holes or slots
- Excellent adhesion to thin film gold and other metals
- Low outgassing
- Excellent thermal stability
- Superior thermal resistance, unaffected by typical assembly temperatures (up to 320 °C)
- Excellent insulator
- Excellent resistance to many solvents
- Lower cost

Property	Value
Hardness	> 75 shore D
Dielectric constant	3.8
Coefficient of thermal expansion	40 x 10^{-6} in/in °C
Via planarity	Flush to 50 % recessed
Allowable hole diameters	Use plated through-hole and slot guidelines

Solder Dams

Solder dams are areas of non-solderable material that are applied to the patterned traces of a thin film circuit in order to prevent solder from flowing away from surface-mounted components during solder reflow. Unwanted solder flow will cause surface-mounted components to move during soldering and also cause solder joints to be thinner and / or weak. There are two types of solder dams that VUSI offers in thin film technology:

- **Polyimide Solder Dams:** Photo-definable polyimide can be used as a solder dam. This polyimide is non-conductive and the typical thickness of the polyimide is 3 µm to 4 µm
- **Metal Layer Solder Dams:** Oxidizing metals like 1 000 Å TiW or 1000 Å Ni are also used as solder dams. The metal solder dam structures are deposited on top of the Au conductors by sputtering and then are patterned. Then the metal is oxidized so it will not wet to solder



Oxidized TiW Solder dam on BeO device

ENEPIG – The Universal Finish

These days, a common challenge in high density thin film circuit design and manufacturing is balancing the competing needs of gold wire bonding and surface-mount soldering on the same circuit. Gold wire bonding processes typically require a minimum of 80 µin of gold in order to form high strength, reliable wire bonds. But most solder mount processes suffer from reduced solder joint strength (embrittlement) at these gold thicknesses due to dilution of the solder by gold. Thinner gold will help reduce solder embrittlement but will create wire bonding problems.

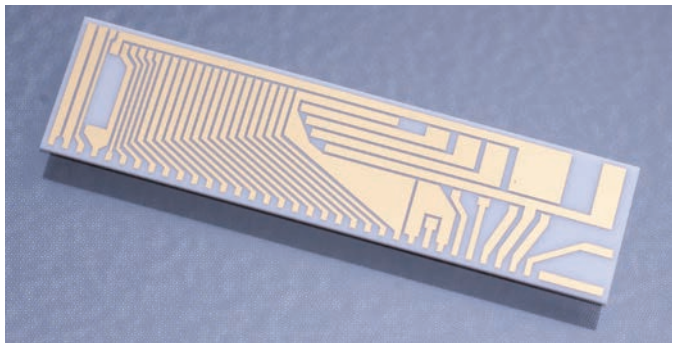
A combination of electroplated films developed by the PCB industry, known as ENEPIG, is a surface finish system that is compatible with both gold and aluminum wire bonding, but also provides high strength soldering. ENEPIG eliminates reliability issues related to gold embrittlement. This finish can now be applied to circuits fabricated by VUSI, thus providing the ultimate flexibility in assembly techniques while maintaining the quality and reliability of a traditional thin film circuit.

ENEPIG is the acronym for electroless nickel (**EN**) electroless palladium (**EP**) immersion gold **(IG**). ENEPIG, defined in specification IPC-4556,* has been adopted as a standard plating scheme for applications including soldering, wire bonding, and as a contact finish.

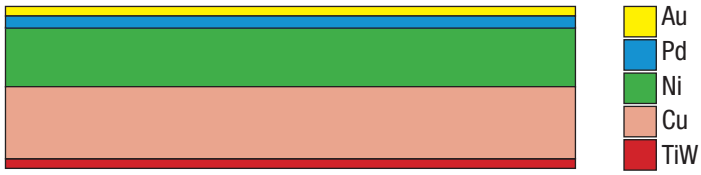
*IPC is the Institute for Interconnecting and Packaging Electronic Circuits.

In the ENEPIG metalization scheme, the palladium inhibits nickel diffusion into the gold layer, promoting long term shelf life before assembly. During soldering, the electroless palladium provides excellent solderability and can withstand multiple rework cycles. The bonding strength of many solders to ENEPIG is very high. Both gold and aluminum wire bonding can be performed directly to ENEPIG.

VUSI has developed a thin film based ENEPIG process that now combines low cost sputtering, traditional thin film photolithography and etching, and plating with ENEPIG. The process is well suited to volume applications. Because the ENEPIG finish is plated and contains very small amounts of precious metal, it is intrinsically less expensive than traditional thin film production choices for providing wire bonding and soldering on the same circuit.



ENEPIG Layer	Thickness
Immersion gold	1.2 µin min.
Electroless palladium	2 µin – 12 µin
Electroless nickel	120 µin – 240 µin
Copper	160 µin – 240 µin (typical)



Cross-section of sputtered copper with plated ENEPIG

Multilayer Possibilities

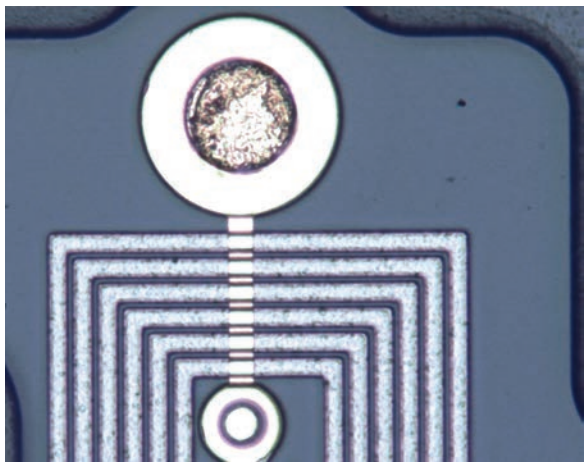
Using multiple polyimide and gold conductor layers, the thin film multilayer solution went into production in 2005 as a reproducible technology that enables the realization of three dimensional DC, RF, and microwave structures. This technology can provide competitive advantages for designers looking to reach new levels of functional density, performance, and miniaturization.

VUSI can provide anywhere from two to nine conductor layers (which are insulated by cured polyimide layers) in order to enable high density circuit designs. The cured polyimide is an excellent medium for sputtering and patterning and is the key enabler of this technology.

Customers who have successfully used this advanced technology have typically generated their design knowledge by building and testing a series of controlled prototypes. UltraFAST can be very helpful for fabricating prototypes quickly. Customers who have embraced this technology have been able to redesign entire product lines and shrink the size of their modules by up to 5x.

The properties of polyimide are presented in the table in the polyimide section above.

Property	Value
Tensile strength	200 MPa
Elongation	45 %
Young's modulus	3.5 GPa
Water absorption	1.3 %
Tg value (TMA)	325 °C
CTE	35 ppm
Dielectric constant	3.3
Dissipation factor	0.001
Dielectric strength	250 kV/mm
Volume resistivity	2.5 x 10^{16} Ω/cm



Spiral inductor under the polyimide, connection to inside of inductor is on top of the polyimide.

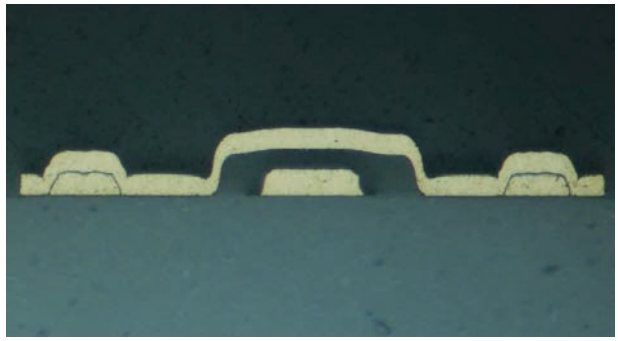
Polyimide-Supported Crossovers

Polyimide-supported crossovers are used to provide permanent crossover connections in structures like Lange couplers. Because the crossover height, length, and placement can be consistently and reliably fabricated, high frequency performance is consistent and repeatable, minimizing testing and tuning time.

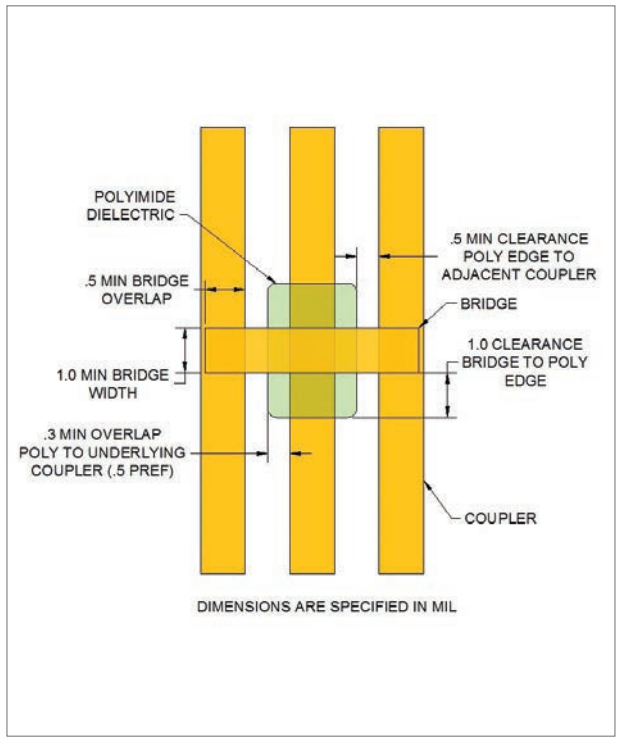
Polyimide-supported crossovers offer improved performance over wire bonds because the crossover connections are fully supported by 3 µm to 4 µm thick polyimide pads. The high temperature cured polyimide pads keep the crossover connections from collapsing or moving, and thus prevent undesirable electrical shorts.

Polyimide-supported crossovers will reduce assembly time and improve assembly yields by eliminating traditional wire bond methods.

The general design guidelines for polyimide-supported crossovers is shown in the picture to the right.



Cross-section of space-qualified polyimide-supported crossover

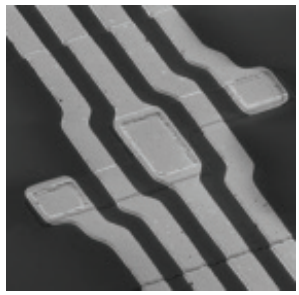


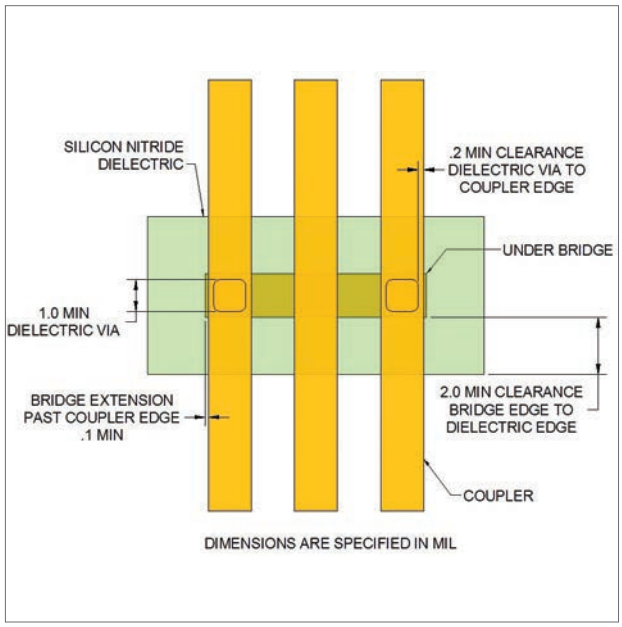
UltraBridge

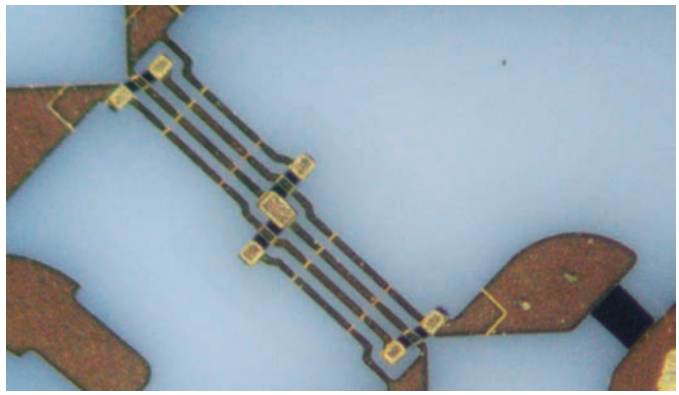
UltraBridge is an innovative solution developed by VUSI to avoid the inherent problems related to wire bonds and Lange couplers. In this specially developed process, the interconnect conductor layer is applied and patterned right on the substrate surface. Silicon nitride (Si_3N_4) is then applied as an encapsulation layer on top of the interconnect layer and then patterned and etched. Contact windows in the silicon nitride layer are then patterned and etched. A final standard thin film layer is then applied on top of the silicon nitride structures. The result is a durable, consistent interconnect solution that can be used to replace fragile air bridges or inconsistent wire bonds.

Because of the purity and resolution possible when processing silicon nitride, UltraBridge offers finer resolution and more consistent processing than polyimide supported crossovers. The hardness of the silicon nitride layer creates a very robust interconnect design unaffected by accidental compression during inspection or assembly.

The general design guidelines for UltraBridge are shown to the right.



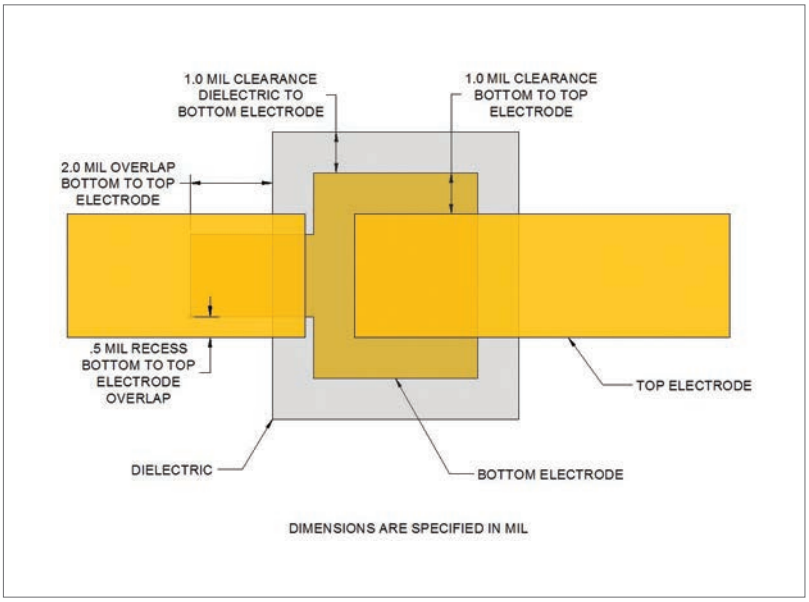


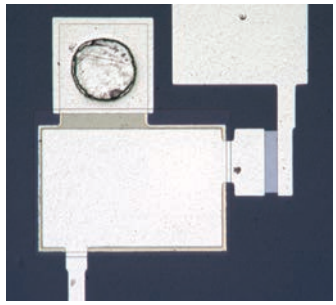


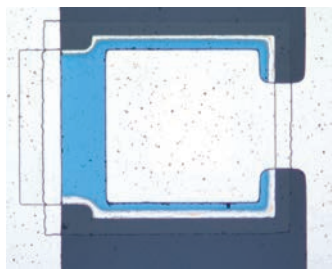
Typical UltraBridge Lange coupler

UltraCapacitor

USI's thin film integrated capacitors are called UltraCapacitors and they are fabricated by using a metal insulator metal (MIM) methodology with a silicon nitride dielectric and thin film sputtered gold electrodes. The UltraCapacitor uses a unique construction methodology in order to avoid the step coverage issues that have inhibited successful production use of thin film capacitors for many years. These thin film capacitors can be integrated into circuit designs where they offer the advantages of solid-state integration, small size, high Q, and reduced assembly requirements. Several customers have also designed their own custom high frequency chip capacitors that we build for use in critical design challenges. A typical UltraCapacitor layout that shows important design considerations is presented below.







Parameter	Values
Dielectric constant	~ 7.2
Dielectric thickness	5000 Å
Capacitance density	0.082 pF/mil^2 (127 pF/mm^2)
Standard values	5 pF – 100 pF
Standard tolerances	± 10 % (> 50 pF), ± 20 % (< 50 pF)
Breakdown voltage	16 V – 30 V (design specific)
Substrate materials	Polished 99.6 % alumina or AlN

UltraCapacitor Layout Details	Values
Bottom electrode metals	TiW (500 Å) / Au (3000 Å)
Bottom electrode minimum pad	2 mils larger than top electrode
Top electrode metals	Standard thin film
Top electrode minimum pad	3 mils x 3 mils (76 µm)