



Meet the Demands of High-Temperature Applications With Thin Film Resistors

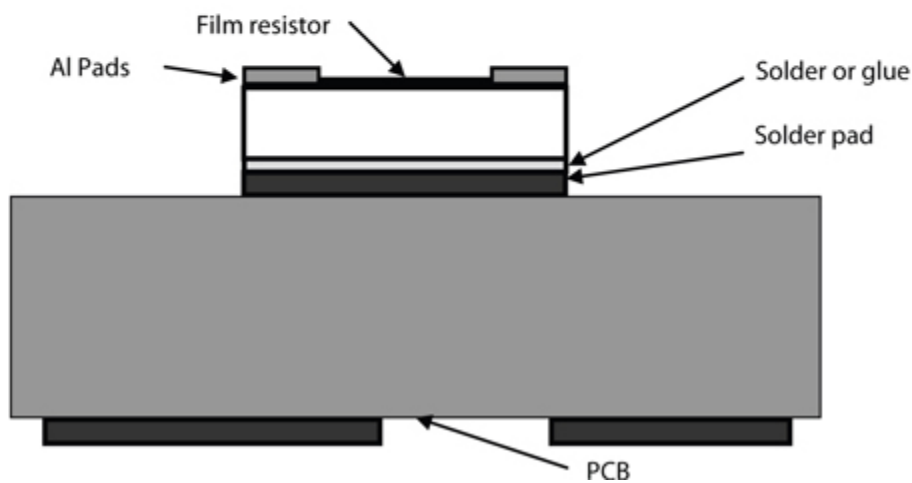
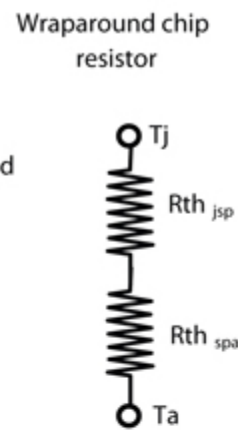
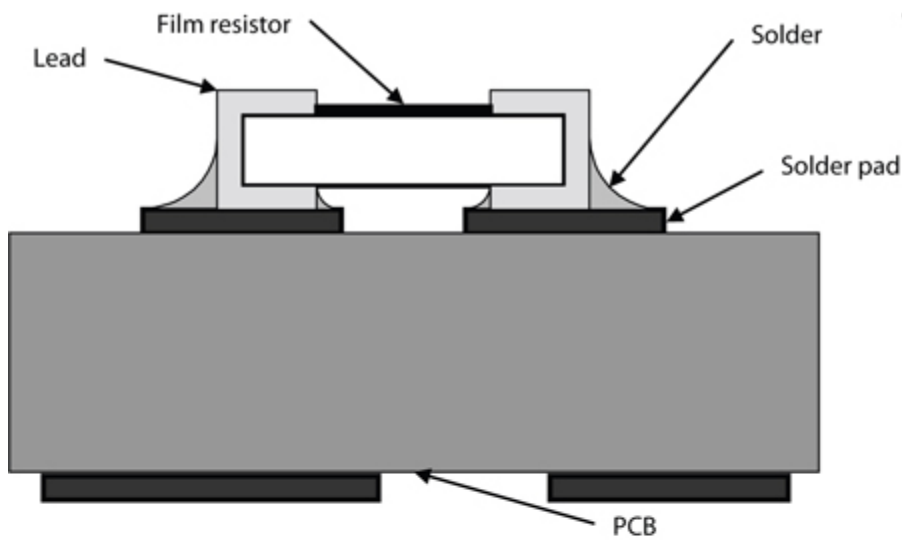
By Dr. Claude Flassayer, Vishay/Sfernice Thin Film Division, www.vishay.com | Thursday, September 30, 2010

The demands in high-[temperature](#) applications are growing more stringent, not only in terms of ambient temperatures up to + 230 °C, but also regarding density of power dissipation and reliability. In order to cope with these severe requirements, a great deal of attention must be paid to controlling the junction and solder joint temperatures to minimize reversible and irreversible resistance drifts.

Thermal Model

In this article, we will explore two types of surface-mounted thin film resistors:

- Wraparound chip resistors and arrays that can be assembled by solder reflow or conductive glues
- Bare chip resistors and networks intended to be wire bonded



In miniaturized surface-mounted components, the heat generated within the resistor is removed to the surrounding environment in the following way:

- Conduction from the resistive layer, or junction, through the body of the chip to the solder pads
- Spreading by conduction within the PCB
- Convection from the PCB to the ambient

Below is a very simple but well recognized model where:

- T_j is the temperature of the resistive layer, or junction
- T_a is the ambient temperature around the PCB
- T_{sp} is the temperature of the solder pad, underneath the solder joint
- P_d is the power dissipation of the resistor
- $R_{th_{ja}}$ is the [thermal](#) resistance between the resistive layer and the ambient
- $R_{th_{jsp}}$ is the thermal resistance between the resistive layer and the solder joint
- $R_{th_{spa}}$ is the thermal resistance between the solder joint and the ambient
- $R_{th_{spa}}$ takes into account the conduction within the PCB and the convection from the PCB to the ambient

Component manufacturers can only take care of $R_{th_{jsp}}$; the control of all others parameters, namely T_a , P_d , and $R_{th_{spa}}$, are addressed by the customer's assembly designers. Designers have to take into consideration the PCB material, the thickness and the layout of the copper tracks, the cooling system, and the interaction between surrounding components.

A poor thermal management might induce:

- Melting of the solder joints
- Lack of reliability of the solder joints
- Loss of PCB performance, even burn out
- Loss of chip resistor performance, mainly due to high reversible or irreversible drifts

Thermal Data

In order to allow designers to use the above thermal model, we shall provide them with:

- Rth jsp for standard parts and enlarged terminations parts
- Experimental data relevant to chip resistors of standard sizes mounted on various PCBs

Meanings of the abbreviations for the data below are:

- PCB sCu: 1.6 mm thick, double sided, 35 μm thick copper (minimum), and at least 50 % copper coverage on both sides
- PCB Mcu: 1.6 mm thick, double sided, 70 μm thick copper (minimum), and at least 80 % copper coverage on both sides
- MCM: Alumina substrates with thick film metallization and at least 50 % conductor coverage. It is equivalent to MCu for the thermal dissipation
- W/A: Enlarged wraparounds equipped with bottom metallization covering their backside, with the exception of a 0.5 mm width insulation path

The following tables show the thermal resistances relevant to various combinations of components and PCBs.

Soldered STD W/A			
Size	Rth _{jsp} (°C/W)	PCB sCu	PCB Mcu
		Rth _{ja} (°C/W)	Rth _{ja} (°C/W)
0603	27	200	67
1206	20	110	60
2010	12	95	52
2512	11	95	51

Soldered Enlarged W/A			
Size	Rth _{jsp} (°C/W)	PCB sCu	PCB Mcu
		Rth _{ja} (°C/W)	Rth _{ja} (°C/W)
1206	5	95	45
2010	2	85	42
2512	1	85	41

Glued STD W/A			
Size	Rth _{jsp} (°C/W)	PCB sCu	PCB Mcu
		Rth _{ja} (°C/W)	Rth _{ja} (°C/W)
1206	33	123	73
2010	18	101	58
2512	16	100	56

Wire Bonding on Back Side Soldered Chip Resistor			
Size	Rth _{jsp} (°C/W)	PCB sCu	PCB Mcu
		Rth _{ja} (°C/W)	Rth _{ja} (°C/W)
1206	5	95	45
2010	2	85	42
2512	1	85	41

Wire Bonding on Back Side Glued Chip Resistor			
Size	Rth _{jsp} (°C/W)	PCB sCu	PCB Mcu
		Rth _{ja} (°C/W)	Rth _{ja} (°C/W)
1206	10	100	50
2010	4	87	44
2512	2	86	42

Derating Curve

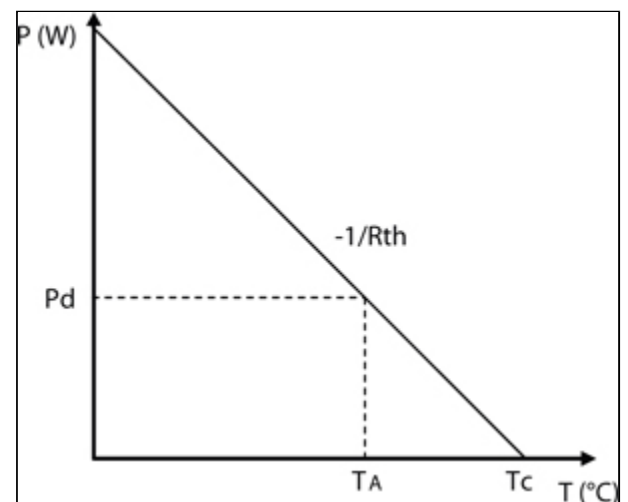
Meaningful Derating Curve

This derating curve is a representation of a basic thermal model:

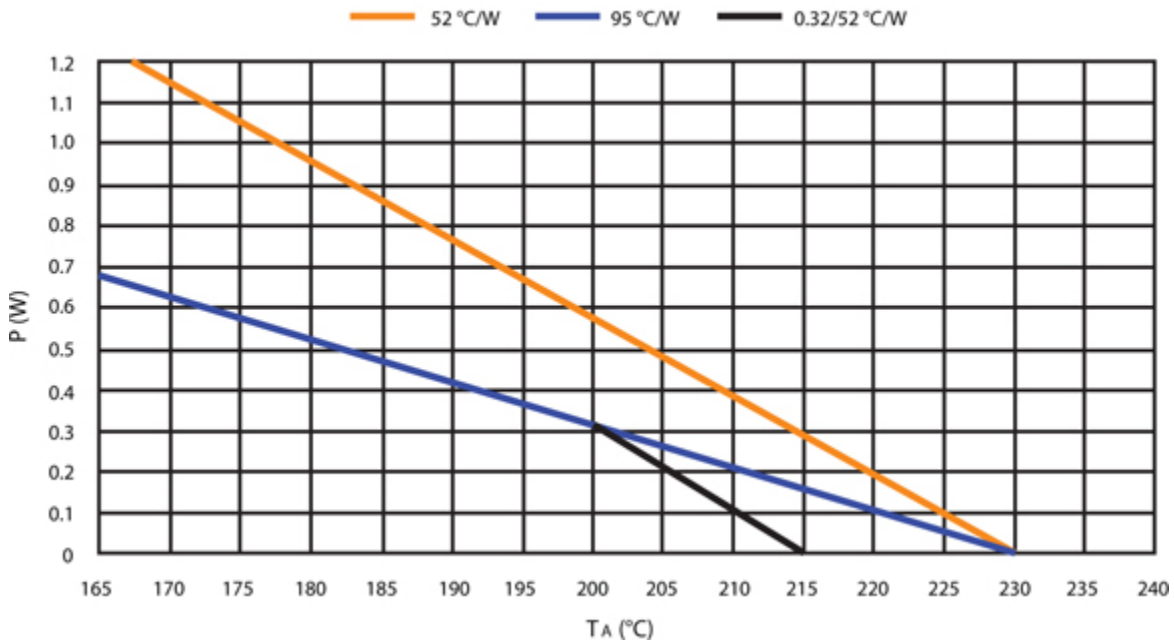
- $T_c = T_a + R_{th} \times P_d$
- T_c = Temperature to be controlled
- T_a = Ambient temperature
- P_d = Maximum allowed power dissipation
- R_{th} = Thermal resistance between point “c” at temperature T_c , and the ambient

It can be written: $P_d = (T_c - T_a)/R_{th}$.

This thermal model gives the maximum allowed P_d for a given T_a , and a specified thermal path characterized by R_{th} . Such a derating curve is used to control T_j , and in this case one considers T_j as T_c , and $R_{th\ ja}$ as R_{th} . It can also be used to control T_{sp} , which is also of premium importance. In this case $T_{sp} = T_c$ and $R_{th} = R_{th\ spa}$.



Example of derating curve (P 2010)



Per the table:

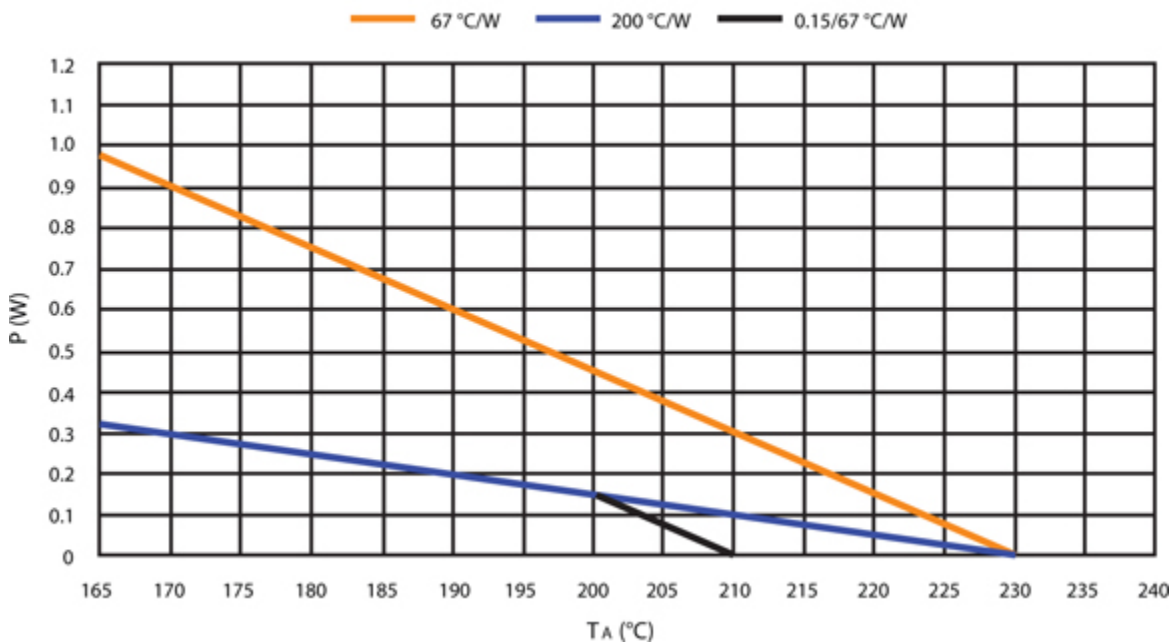
- Rth ja = 52 °C/W (P 2010 on a MCu PCB)
- Rth ja = 95 °C/W (P 2010 on a sCu PCB)

There are different ways to use this derating curve. Providing Tj max = + 230 °C, the maximum power dissipation of the resistor at Ta = + 200 °C will be:

- 0.57 W for Rthp= 52 °C/W (best assembly)
- 0.32 W for Rthp= 95 °C/W (standard assembly)

From the same derating curve one can see that a 0.32 W power dissipation on the best assembly (Rth ja = 52 °C/W) will limit Tj at + 215 °C, and therefore decrease the resistance drift thoroughly.

Example of derating curve (P 0603)



- Rth ja = 67 °C/W (P 0603 on a MCu PCB)

- $R_{th\ ja} = 200\text{ }^{\circ}\text{C/W}$ (P 0603 on a sCu PCB)

Providing $T_j\ \text{max} = +230\text{ }^{\circ}\text{C}$, the maximum power dissipation of the resistor at $T_a = +200\text{ }^{\circ}\text{C}$ will be:

- 0.447 W for $R_{thp} = 67\text{ }^{\circ}\text{C/W}$ (best assembly)
- 0.15 W for $R_{thp} = 200\text{ }^{\circ}\text{C/W}$ (standard assembly)

Conclusion

To help assembly designers keep T_j under control, we have worked out a thermal model and have shown the thermal resistance figures necessary to use this model. From there we defined and displayed some derating curves, which illustrate how good thermal management leads to load-life drift minimization. The next step will be for manufacturers to improve their design and process in order to push away the $+230\text{ }^{\circ}\text{C}$ T_j limitation.

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