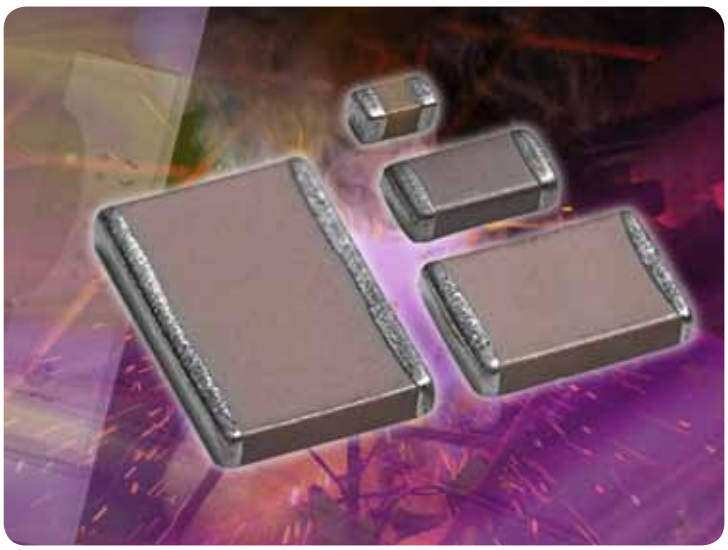
Capacitors - Excellent Reliability

Open-Mode Design MLCC Capacitors



KEY BENEFITS

- Reduces the risk of shorts or low insulation resistance (IR) due to board-flex cracks
- Available with polymer terminations for intensive board flex requirements
- Features higher voltage breakdowns than standard designs with voltage ranges from 16 V_{DC} to 3000 V_{DC}
- Provides high-frequency filtering for switching power supplies
- Available with 100 % voltage condition

APPLICATIONS

- Buck and boost DC/DC converters
- Voltage multipliers for flyback converters
- High-frequency filtering in power supplies for medical, computer, motor control, and telecommunications systems

RESOURCES

- Datasheet: VJ OMD Series - http://www.vishay.com/doc?45198
- For technical questions contact mlcc@vishay.com
- Material categorization: For definitions of compliance please see http://www.vishay.com/doc?99912

RoHS COMPLIANT HALOGEN FREE

One of the World's Largest Manufacturers of
Discrete Semiconductors and Passive Components

Surface Mount Multilayer Ceramic Chip Capacitor Solutions for Boardflex Sensitive Applications

ELECTRICAL SPECIFICATIONS

C0G (NP0)

GENERAL SPECIFICATION

Note
Electrical characteristics at + 25 °C unless otherwise specified

Operating Temperature: - 55 °C to + 125 °C

Capacitance Range: 10 pF to 47 nF

Voltage Range: 50 V_{DC} to 3000 V_{DC}

Temperature Coefficient of Capacitance (TCC):
0 ppm/°C ± 30 ppm/°C from - 55 °C to + 125 °C

Dissipation Factor (DF):
0.1 % maximum at 1.0 V_{RMS} and 1 MHz for values ≤ 1000 pF
0.1 % maximum at 1.0 V_{RMS} and 1 kHz for values > 1000 pF

Insulating Resistance:
At + 25 °C 100 000 MΩ min. or 1000 ΩF whichever is less
At + 125 °C 10 000 MΩ min. or 100 ΩF whichever is less

Aging Rate: 0 % maximum per decade

Dielectric Strength Test:
Performed per method 103 of EIA 198-2-E
Applied test voltages

≤ 200 V_{DC}-rated:	250 % of rated voltage
500 V_{DC}-rated:	200 % of rated voltage
630 V_{DC}/1000 V_{DC}-rated:	150 % of rated voltage
1500 V_{DC} to 3000 V_{DC}-rated:	120 % of rated voltage

X7R

GENERAL SPECIFICATION

Note
Electrical characteristics at + 25 °C unless otherwise specified

Operating Temperature: - 55 °C to + 125 °C

Capacitance Range: 100 pF to 1.8 µF

Voltage Range: 16 V_{DC} to 3000 V_{DC}

Temperature Coefficient of Capacitance (TCC):
± 15 % from - 55 °C to + 125 °C, with 0 V_{DC} applied

Dissipation Factor (DF):
< 50 V ratings 3.5 % maximum at 1.0 V_{RMS} and 1 kHz
≥ 50 V ratings 2.5 % maximum at 1.0 V_{RMS} and 1 kHz

Insulating Resistance:
At + 25 °C 100 000 MΩ min. or 1000 ΩF whichever is less
At + 125 °C 10 000 MΩ min. or 100 ΩF whichever is less

Aging Rate: 1 % maximum per decade

Dielectric Strength Test:
Performed per method 103 of EIA 198-2-E
Applied test voltages

≤ 250 V_{DC}-rated:	250 % of rated voltage
500 V_{DC}-rated:	min. 150 % of rated voltage
630 V_{DC}/1000 V_{DC}-rated:	150 % of rated voltage
1500 V_{DC} to 3000 V_{DC}-rated:	120 % of rated voltage

ORDERING INFORMATION

VJ1210	Y	474	J	X	A	A	T	# [2]
CASE CODE	DIELECTRIC	CAPACITANCE NOMINAL CODE	CAPACITANCE TOLERANCE	TERMINATION	DC VOLTAGE RATING [1]	MARKING	PACKAGING	PROCESS CODE
0805 1206 1210 1808 1812 1825 2220 2225	A = C0G (NP0) Y = X7R	Expressed in picofarads (pF). The first two digits are significant, the third is a multiplier. An "R" indicates a decimal point. **Examples** 474 = 470 000 pF	F = ± 1 % G = ± 2 % J = ± 5 % K = ± 10 % M = ± 20 % **Note** C0G (NP0): F, G, J, K X7R: J, K, M	X = Ni barrier 100 % tin plated matte finish F, E = AgPd [3] B = Polymer 100 % tin plated matte finish N = Non-magnetic	J = 16 V X = 25 V A = 50 V B = 100 V C = 200 V P = 250 V E = 500 V L = 630 V G = 1000 V R = 1500 V F = 2000 V H = 3000 V	A = Unmarked	C = 7" reel/paper tape T = 7" reel/plastic tape P = 11 1/4"/13" reel/ paper tape R = 11 1/4"/13" reel/ plastic tape O = 7" reel/flamed paper tape **Note** "I" and "O" are used for "F", "E" termination size 0805	4X = OMD cap 5H = OMD cap 100 % voltage conditioning

Notes
[1] DC voltage rating should not be exceeded in application. Other application factors may affect the MLCC performance. Consult for questions: mlcc@vishay.com
[2] Process code with 2 digits has to be added.
[3] Termination code E" is for conductive epoxy assembly.

BOARDFLEX SENSITIVE APPLICATIONS - SOLUTION:

A predominant failure mode in multilayer ceramic chip capacitors is cracking caused by board flexure. Cracks can then create a path for current to pass from one electrode through the dielectric to an opposing electrode or from the terminations at one end of the MLCC through the dielectric to an opposing electrode. This may subsequently result in capacitance loss, leakage - low Insulation Resistance (IR) - and/or more seriously, high current shorts. A short circuit condition in the surface mounted capacitors can cause further failures of downstream components. Vishay's Open Mode Design Capacitors (VJ OMD - Cap. series) reduce the risk of these destructive conditions through MLCC designs that prevent board flexure cracks reaching the opposing electrode.

VJ OMD - Cap. MLCCs reduce the risk of early field failures associated with board flex cracks. However, it is important to note that even in the open mode designs the presence of flexure related cracks can cause capacitance loss leading to localized stresses on the parts. eventually, depending on the application environment, including such factors and high voltage pulse frequency and thermal cycling this may lead to internal breakdown of the component.

POLYMER TERMINATION

Polymer termination provides additional protection against board flexure damage by absorbing greater mechanical and thermal stresses. Components can be packaged, transported, stored and handled the same standard terminated product. Wave and reflow soldering of MLCC does not require modification to equipment and/or process. Polymer termination greatly reduces the risk of mechanical cracking however it does not completely eliminate.

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