Resistive Products

Application Note

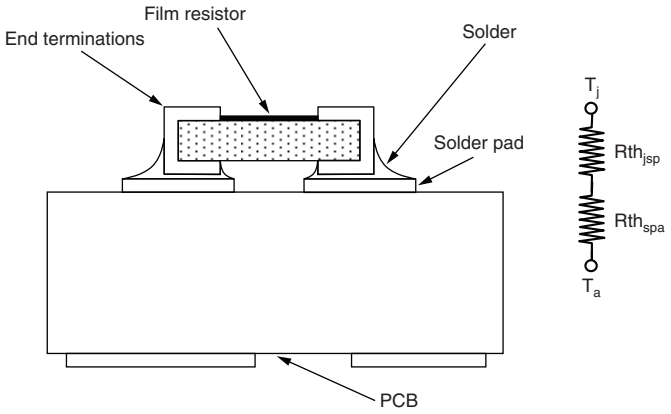
Power Dissipation in High Precision Vishay Sfernice Chip Resistors and Arrays (P Thin Film, PRA Arrays, CHP Thick Film)

A. ABSTRACT

Datasheets for surface-mount components in general and for chip resistors and arrays in particular tend to offer very limited information on thermal performance. Typically they provide derating curves that are similar to the ones used for through-hole components, even though the respective heat dissipation properties of these two component types are quite different. In the larger, leaded components, heat dissipation occurs mainly by direct convection and radiation from the component to the ambient. Only a small portion of the heat is dissipated by conduction through the leads and PCB and then by convection and radiation to the ambient. Thus it makes sense to take the component body temperature as a basis for determining by how much the power needs to be derated when this temperature increases. In smaller surface-mount components such as Vishay's thin film chip resistors and arrays, by contrast, more than 90 % of the heat, is dissipated from the body of the component directly into the solder pad, from there to the PCB, and thence by convection to the ambient.

Unfortunately the only specifications on the datasheet that are key to the thermal management process are the maximum junction temperature and internal thermal resistance. Everything else depends on the system design, including the ambient temperature, cooling system, thermal behavior of the PCBs, maximum temperature of the solder joints, and so forth. This application note provides designers with addtional guidance on how to get the best performance from high-precision thin film chip resistors and arrays from a thermal management point of view.

B. THERMAL MODEL



On miniaturized surface-mount-components the heat generated within the resistor is dissipated to the surrounding environment in the following way:

- Conduction from the resistive layer, or junction, through the body of the chip, to the solder pads
- Spreading by conduction within the PCB
- Convection from the PCB to the ambient

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The components are so small compared to the PCB that heat removal by direct convection and/or radiation from the resistor body is ignored in the following simple but well recognized model:

1. $T_j = T_a + Rth_{ja} \times Pd = T_a + (Rth_{jsp} + Rth_{spa}) \times Pd = T_a + Rth_{jsp} \times Pd + Rth_{spa} \times Pd$

2. $T_{sp} = T_a + Rth_{spa} \times Pd$

where

- T_j is the temperature of the resistive layer, or junction
- T_a is the ambient temperature around the PCB
- T_{sp} is the temperature of the solder pad, underneath the solder joint, it is almost equal to solder joint temperature
- Pd is the power dissipation of the resistor
- Rth_{ja} is the thermal resistance between the resistive layer and the ambient
- Rth_{jsp} is the thermal resistance between the resistive layer and the solder joint
- Rth_{spa} is the thermal resistance between the solder joint and the ambient
- Rth_{spa} takes into account the conduction within the PCB and the convection from the PCB to the ambient

The key thermal resistance value for component manufacturers is Rth_{jsp}, which is affected by the choice of material, the resistor pattern, and the terminations. Manufacturers also strive to improve the thermal stability of their resistors, such that the devices can withstand higher and higher temperatures without undergoing significant drifts, and the maximum junction temperature can be increased. All the other thermal parameters must be addressed by the system designer, who must take into consideration the PCB material, the thickness and the layout of the copper tracks, the cooling system, the interaction between surrounding components, and so forth.

With increasing use of computer-aided design, this is the only way to handle the more and more stringent requirements imposed by miniaturization, higher power density, temperature exposure, reliability, and so forth.
Indeed, there are severe consequences for inadequate thermal management, including melting or unreliability of the solder joints, impaired PCB performance, and impaired resistor performance being caused by too much drift, either reversible or irreversible.
This is why thermal management is so important.

C. DATA

As noted previously, the nominal power and derating information supplied by datasheets is inadequate to allow designers to get the best performance from chip resistors, and sometimes it can even be misleading. This application note provides designers with the Rth_{jsp} for standard and enlarged-termination parts as well as experimental data relevant to chip resistors of standard sizes mounted on various PCB types to allow them to use the thermal model presented above. These PCBs have been chosen to be representative of the worst, typical, and best cases in terms of thermal resistance. The resulting data will help designers who can not calculate thermal resistance by themselves, or to complete their CAD approach.

The Rth_{jsp} values were computed from datasheet information and the following thermal conductivity values:

MATERIAL	THERMAL CONDUCTIVITY ($W \times m^{-1} \times K^{-1}$)
Alumina	25
Cu	400
Ni and SnAg	50
FR4	0.26
AlN	100 up to 200

Table 1 contains all the data necessary to make calculations using the thermal model.

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Table 1

Size	Rth_{jsp} (°C/W)	mCu EN 140401		sCu (Nat) Load life PCB		sCu (1 m/s) Load life PCB		MCu (Nat) Universal PCB		Enlarged Terminations
		Rth_{ja} (°C/W)	Rth_{spa} (°C/W)	Rth_{ja} (°C/W)	Rth_{spa} (°C/W)	Rth_{ja} (°C/W)	Rth_{spa} (°C/W)	Rth_{ja} (°C/W)	Rth_{spa} (°C/W)	Rth_{jsp} (°C/W)
0302	35									
0402	30	870	840							
0505	20									
0603	27	550	523	200	173	120	93	67	40	
0805	23	440	417	136	113			63	40	
1005	25									
1206	20	220	200	110	90	73	53	60	40	5
1505	30									4
2010	12	140	128	95	83	57	45	52	40	2
1020	5									
2512	11	110	99	95	84	36	25			1

(Figures will be added to the blank cells as experimental data is gathered.)

The first columns present Rth values per EN 140401, namely Rth_{ja} and Rth_{spa} , with $Rth_{ja} = Rth_{jsp} + Rth_{spa}$.These very high Rth numbers represent conservative values. As component suppliers cannot know how all components will be used, they tend to publish numbers based on worst-case assumptions. These assumptions include a very poor PCB with a minimal (35 µm) copper coating on one side only; minimum size for the solder pads; and no particular attention to copper tracks and copper coverage (lower than 20 %), as shown in Annex 2, Picture 1 (we will call it mCu).

The same table contains some experimental data relevant to more standard PCBs. By “standard,” we mean a double-sided board with a 35 µm copper layer, at least 50 % copper coverage, and solder pads sized according to datasheet recommendations, as shown in Annex 2, Picture 2 (we will call it sCu).

Such PCBs, which were used for our internal load life tests, have been tested in natural air convection and forced air convection (at 1 m/s) (here called sCu (Nat) and sCu (1 m/s)).

The Rth_{ja} and Rth_{spa} values, even in natural convection, are lower than the figures provided in datasheets and are more representative of what the designer can expect in a normal layout.
Of course, forced air convection will improve thermal conduction and reduce Rth_{ja} and Rth_{spa}.

As for the best-case scenario, we assume the use of a double-sided PCB with a 70 µm copper layer covering more than 80 % of both sides. Equipping these PCBs with ground planes and thermal vias is recommended but not essential to obtain the Rth values shown in the table (we will call them MCu).

For our “Universal PCB” (see Annex 2, Picture 3), we get the same Rth_{spa} regardless of the resistor size. This is because the solder pads are oversized and the copper amount around each position does not change with component size.

For special and very stringent power dissipation requirements, Rth_{jsp} can be reduced using chip resistors with enlarged terminations; these are soldered on large and thick copper pads acting as heat sinks (see Annex 2, Picture 4).
The Rth_{jsp} values for large sizes terminations are also shown in Table 1. Values for other sizes can be computed easily.

We should also note that the use of AlN instead of Al_2O_3 should be reserved for very special applications, particularly when the chip is mounted on a temperature-regulated heat sink.

D. NEW APPROACH FOR DERATING CURVES

First of all it is important to see what pieces of information are contained in the existing surface mount chip resistor derating curves.

- Pn stands for nominal power dissipation, it is the specified maximum power dissipation which can be applied to the component for ambient temperature lower than 70 °C
- The maximum operating temperature the component can withstand, most often 155 °C which is compulsory for military applications
- The reduced power dissipation which is allowed for ambient temperatures above 70 °C and below the maximum operating temperature

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All the derating curves are a representation of a basic thermal model:

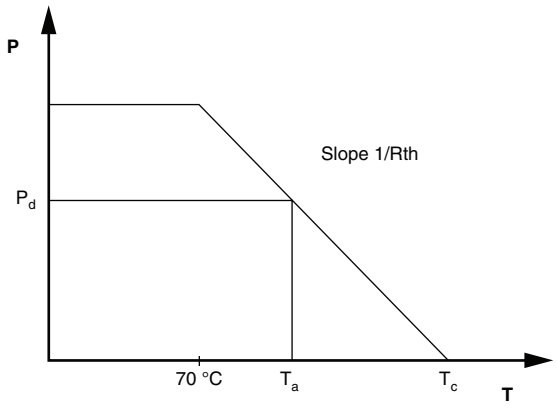
- $T_c = T_a + Rth\ Pd$
- T_c = Temperature to be controlled
- T_a = Ambient temperature
- Pd = Maximum allowed power dissipation
- Rth = Thermal resistance between point “c”, at temperature T_c, and the ambient.

It can be written:

$Pd = (T_c - T_a)/Rth$

This gives the maximum allowed power dissipation, Pd, for a given ambient temperature, T_a, and a specified thermal path characterized by Rth.

This is the derating curve, a straight line with a slope equal to (- 1/Rth), arbitrarily truncated at 70 °C.



There are a lot of misunderstandings regarding this derating curve.

The first one concerns the way it is drawn.
Sometimes marketing engineers take the value of Pn, known through benchmarking, and the most stringent operating temperature for the military applications they intend to serve, 155 °C, and on this basis draw a line from Pn at 70 °C down to 0 at 155 °C. Unfortunately this slope is not a realistic representation.

Fortunately for most applications, the actual Rth of the assembled components is lower than the ones derived from derating curves drawn in this way, and the most negative consequence is that the full capabilities of the components are not realized in the design.
However, in new applications that are more and more demanding in terms of miniaturization, this approach is not acceptable. Typically component design engineers draw the derating curves on the basis of the worst-case assembly conditions. This reduces the risk of problems, but it also means component use is not being optimized.

The second misunderstanding concerns the way the derating curve is used.
Taking the value of Pn at 70 °C is purely a convention, and for temperatures lower than 70 °C, higher levels of power, Pd > Pn, can be dissipated.
One can get Pd simply continuing the straight line, down to the actual ambient temperature, T_a.

A third misunderstanding is relevant to the possibility of increasing Pd by improving the thermal path.
Obviously, if we design a thermal path with a Rth lower than the one coming from the derating curve, it is possible to get a Pd at 70 °C that is higher than Pn.
This is particularly important when it comes to miniaturized electronic assemblies.

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E. UNDERSTANDING THERMAL PATHS

PCB designers working with thermal simulation software can start working with their own data. Such simulations can provide a value for Rth_{spa}, which will allow the designer to control the temperature of the solder pad, which is also the temperature of the solder joint.
(3) $T_{sp} = T_a + Rth_{spa} \times Pd$
As we'll see, T_{sp} is the most important temperature parameter to get under control.

With SnPb solder alloys and FR4 board material, the maximum recommended T_{sp} is 110 °C.
For SnAg solder alloys and special PCBs, this maximum temperature can potentially be increased, up to 150 °C, but there is insufficient data on SnAg solder joints to make this a general rule. What we do know is that the higher the T_a, the less power can be applied. Thus for a given $T_a < T_{sp}$ max. one can find the allowed power dissipation by:
(4) $P = (T_{sp}\ max. - T_a)/Rth_{spa}$
This is the equation of the derating curve relevant to the solder pad.

To obtain the best performance from chip resistors, T_j should also be kept lower than 155 °C.

This is the maximum temperature specified on Vishay datasheets, although for high- temperature applications specially treated devices are available that increase Tj max. up to 200 °C and even higher.
(5) $T_j = T_a + Rth_{jsp} \times Pd + Rth_{spa} \times Pd$
For a given $T_a < T_j$ max. one can get the allowed power dissipation
(6) $P = (T_j\ max. - T_a)/(Rth_{jsp} + Rth_{spa})$

This is the equation of the derating curve relevant to the junction or resistive layer.

The signs of overheating of the solder pads or/and of the PCB material are visible far before any significant drift of the ohmic value can be detected, this means that controlling T_{sp} is a priority.
This also confirms what the thermal model is showing. For the combinations of Pd and Rth_{jsp} that we are dealing with, the thermal gradient between the junction and the solder pad is lower than 20 °C, as Vishay resistors are designed to work optimally at junction temperatures up to 175 °C; thus there is no limitation imposed by T_j.

We will be issuing a special datasheet dedicated to 200 °C applications. Thus, for applications other than 200 °C ones, requiring special assemblies, we will focus on the limitation imposed by T_{sp} max.

For the different chip sizes, we can draw up derating curves from equation (4) taking into account figures from Table 1 and the three typical PCB configurations already discussed, mCu, sCu, and MCu.

This set of curves, (or simple calculations obtained by a worksheet from the basic thermal model) might be helpful for PCB designers not equipped to perform the analyses necessary for accurate thermal management .

Let's consider the respective consequences when T_{sp} max. = 155 °C (equal to T_j max.) and T_{sp} max. = 125 °C.

E.1 T_{sp} max. = 155 °C

For military applications, the assembly and the solder joint can withstand 155 °C, which is the maximum operating temperature. We have provided curves relevant to the most standard sizes (0603, 0805,1206, and 2010) and additional curves can be created from the derating curve equations (4) and (6).
On the graph shown in Annex 1 we can see :

- The datasheet derating curve
- The derating curves relevant to Tsp for "mCu", "sCu", and "MCu"

The equations and the corresponding curves allow some interesting observations.

- For 0603, 0805, and 1206 sizes, and even for the worst-case "mCu" PCB, the "Tsp derating curves" are above those provided on the datasheets; this means that one can apply a higher Pd than specified in the datasheet.
  In fact the Pd at 70 °C can be increased respectively up to 162 mW, 203 mW, and 425 mW
- For the 2010 size, an "sCu" should be used in order to achieve a $T_{sp} < 155$ °C under 1 W. If one has to assemble a P2010 on an "mCu" PCB, the Pd at 70 °C should be reduced down to 0.66 W.

Using an "MCu" PCB, the applied power can be very high compared to Pn.

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E.2 T_{sp} max. = 125 °C

Numerous applications require components with a maximum operating temperature of 125 °C.
The corresponding set of "T_{sp} = 125 °C derating curves" can be drawn very easily from the previous "T_{sp} = 155 °C" ones. Just make a "30 °C" translation .

In this case the remarks are:

- The "T_{sp} derating curves" relevant to "mCu" are below the datasheet ones, this means that this "T_{sp} derating curve" is applicable over the others.
- The Pd at 70 °C must be decreased for the 0603, 0805, 1206 and 2010 sizes respectively down to 103 mW, 132 mW and 390 mW.
- The "T_{sp} derating curves" relevant to "sCu" are partly below and, partly above the datasheet values for the 0603, 0805, and 1206 sizes.
- The cross-over temperatures are respectively 115 °C, 113 °C, and 110 °C
- Above the cross-over temperature, the "T_{sp} derating curve" should be used; below this temperature the same curve can also be used
- For the 2010 size, the "T_{sp} derating curves" relevant to "sCu" are applicable for T_a > 42 °C
- The "T_{sp} derating curves" relevant to "MCu" are partly below, partly above the datasheet ones for sizes 0603, 0805, 1206 and 2010
- The cross-over temperatures are respectively 122 °C, 120 °C, and 87 °C
- Above the crossover temperature, the "T_{sp} derating curve" must be used; below this temperature the same curve can also be used.

Simple translation of these curves will give figures relevant to any value forT_{sp} max.

F. ENLARGED TERMINATIONS FOR LARGEST CHIP SIZE

It is tempting to suppose that the of use larger chips by itself could serve as a solution when more power needs to be dissipated. Calculations and measurements show, this is obviously not the case and a great deal of attention should be paid to the thermal management of the largest chip resistors.
One way to optimize real estate is to use enlarged terminations together with a high power dissipating PCB, such as the MCu type.
As Table 1 shows the main limitation comes from Rth_{spa}.
Therefore the T_{sp} derating curves are quite easy to draw.
$Pd = (T_{sp} - T_a)/(Rth_{spa} + Rth_{jsp})$
And the result is a straight line starting from $T_{sp\ max.}$, with a slope roughly equal to (- 1/40) W/°C.

G. CONCLUSION

On the basis of a simple but well recognized thermal model we have shown that T_{sp}, the temperature of the solder pad, is the most important temperature parameter that needs to be controlled in order to get the best performance from chip resistors and arrays.
Components designers are working to

- Increase the maximum allowed temperature junction: T_j
- Reduce the internal thermal resistance: Rth_{jsp}
- Improve the thermal stability of the internal layers

As a consequence T_{sp} is most often the limiting parameter and therefore, the importance of controlling T_{sp} is more important than ever.

Thermal management through T_{sp} control is the task of assembly design engineers. To help them in this task we have compiled and provided the experimental data included in this application note.

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Highlights from this compilation are:

1. If T_{sp} max. = 155 °C is acceptable for the solder joint, and for the PCB, integrity and reliability, then:

- Worst case “mCu” PCBs can be used without any power derating in excess of the value indicated by the datasheet, except for P2010 devices (see curve).
- Pd can be slightly higher than Pn at T_a = 70 °C.
- For T_a < 70 °C a higher Pd is acceptable, and can be derived from the T_{sp} derating curve.
- At a minimum standard “sCu” PCBs should be used with P2010.
- For smaller sizes “sCu” assembly allows a higher Pd than specified.
- “MCu” PCBs allow an even higher Pd.

2. If T_{sp} max. = 125 °C, the following guidelines should be followed to ensure solder joint reliability:

- For “mCu” PCBs, the T_{sp} derating curve is applicable
- For “sCu” PCBs, the T_{sp} derating curve will reduce Pd for T_a > 110 °C and will allow a higher Pd for T_a < 110 °C (for P2010, the T_{sp} derating curve is applicable)
- For “MCu” PCBs, the T_{sp} derating curve will reduce Pd for T_a > 120 °C and will allow higher Pd for T_a < 120 °C (for P2010, the T_{sp} derating curve is applicable)

3. Enlarged terminations chips mounted on “MCu” PCBs allow for better power dissipation, and represent an interesting solution for large size chips. The T_{sp} derating curve, with a Rth_{spa} close to 40 °C/W, is applicable.

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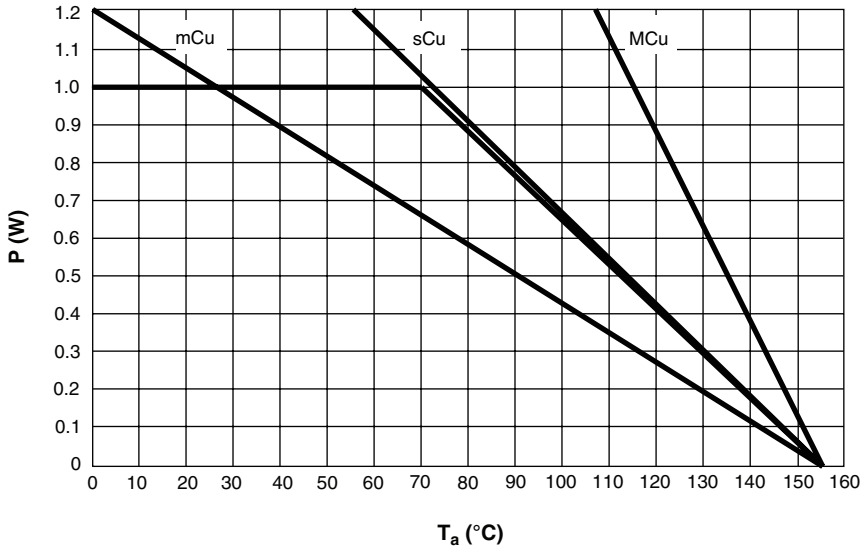
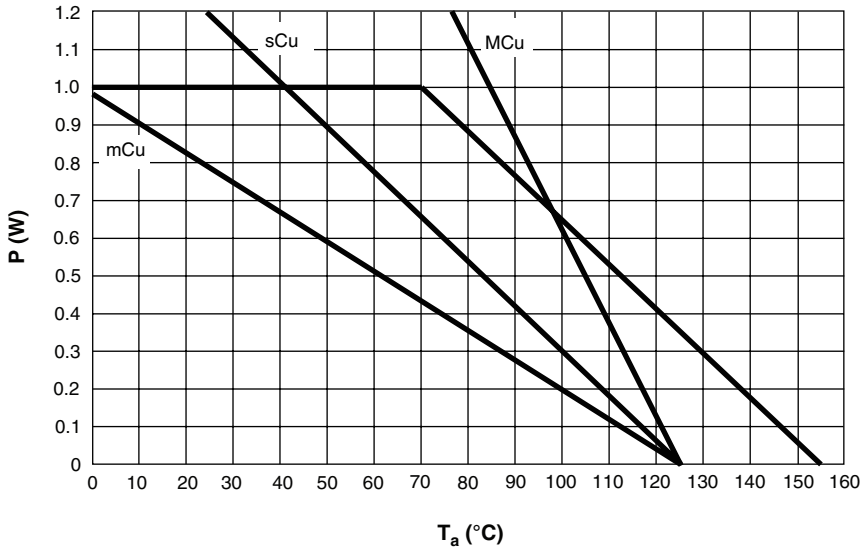
ANNEX 1 - DERATING CURVES

P2010 - T_{sp} max. = 155 °C



P2010 - T_{sp} max. = 125 °C



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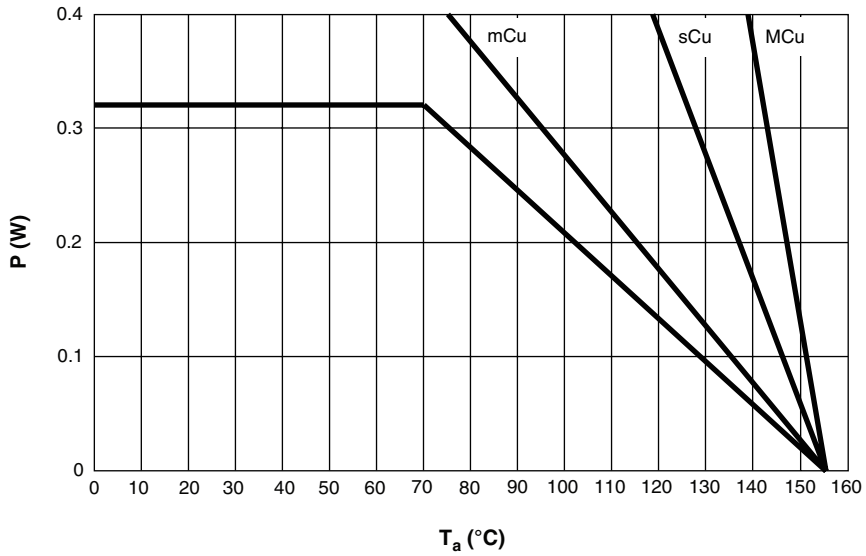
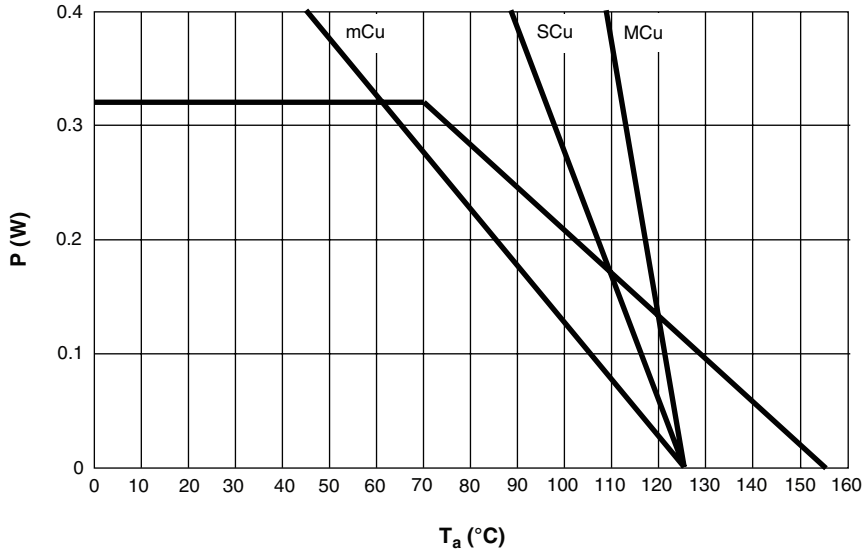
P1206 - T_{sp} max. = 155 °C



P1206 - T_{sp} max. = 125 °C



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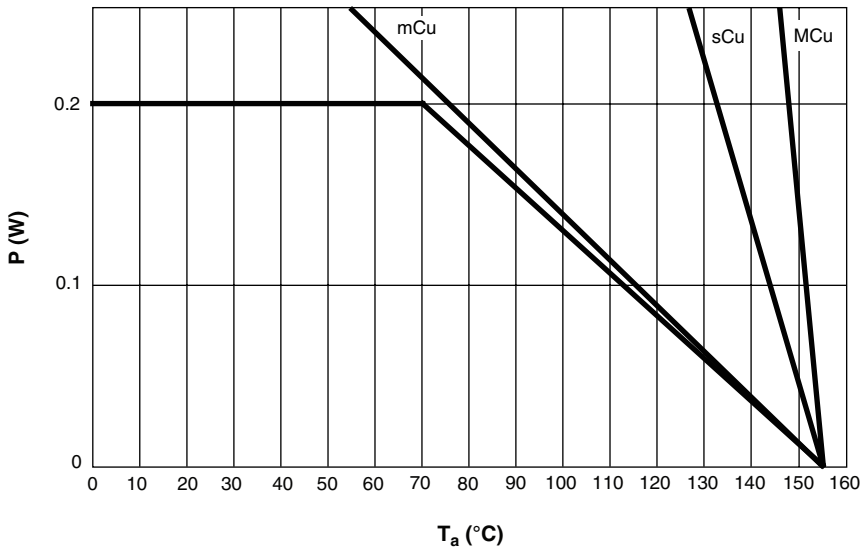
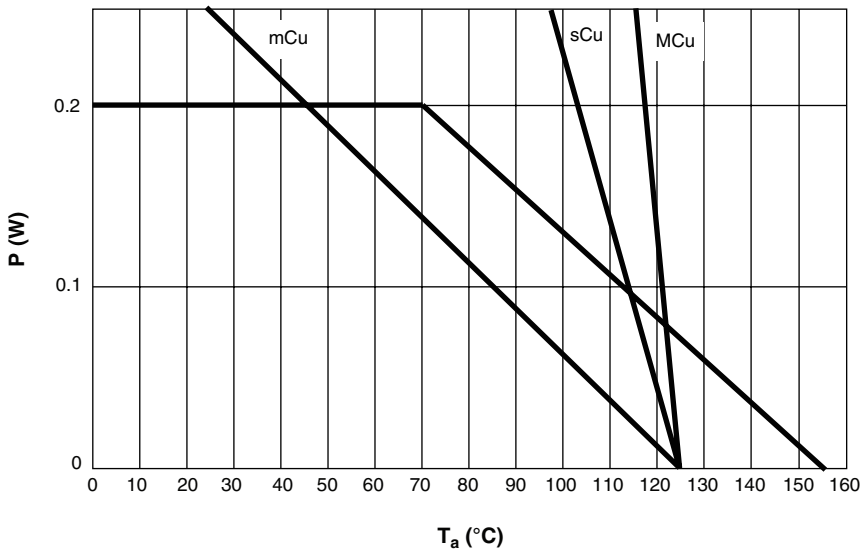
P0805 - T_{sp} max. = 155 °C



P0805 - T_{sp} max. = 125 °C



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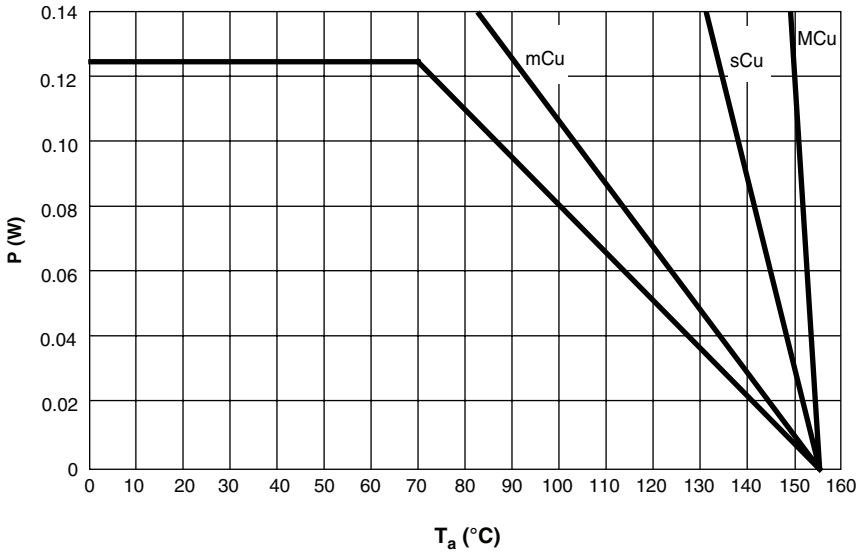
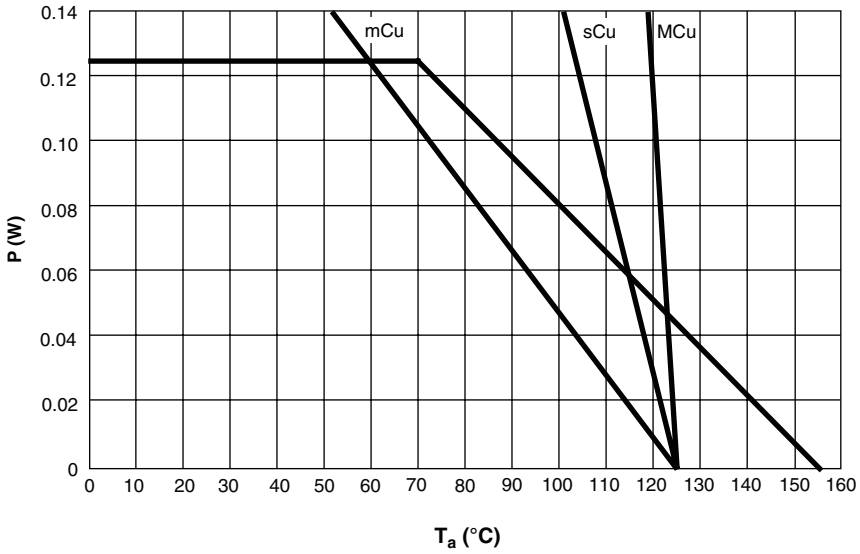
P0603 - T_{sp} max. = 155 °C



P0603 - T_{sp} max. = 125 °C



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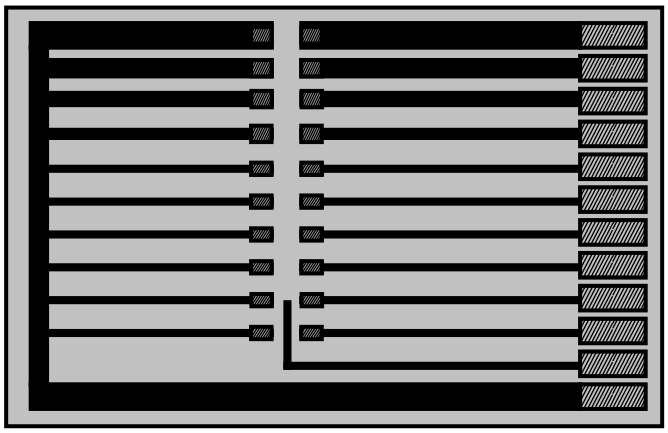
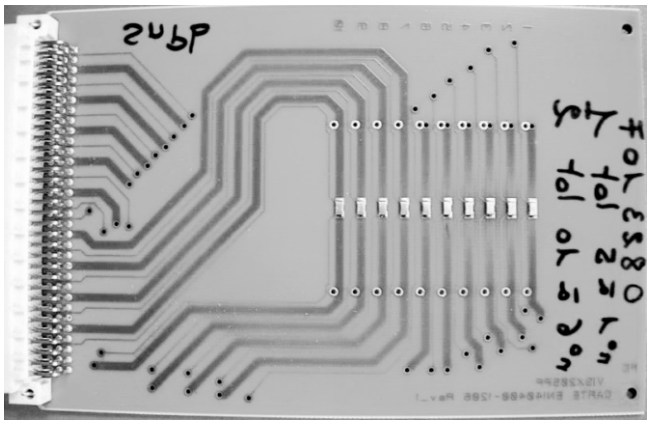
ANNEX 2 - PCB CONFIGURATIONS

Picture 1
mCu PCB (EN140401)

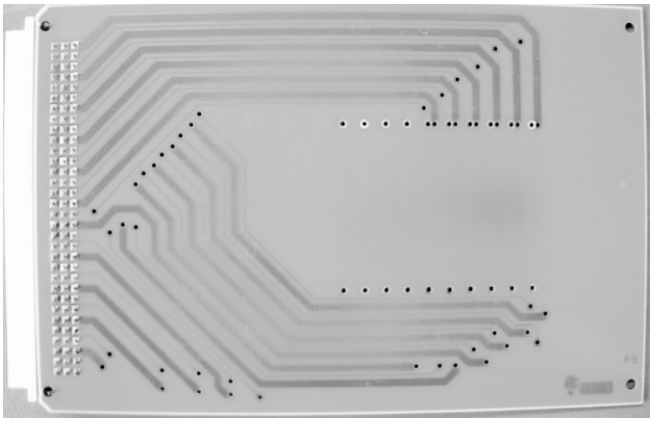


Picture 2
sCu PCB

Front view



Rear view



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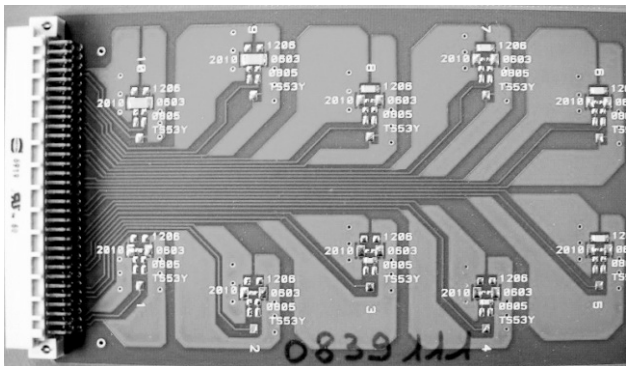
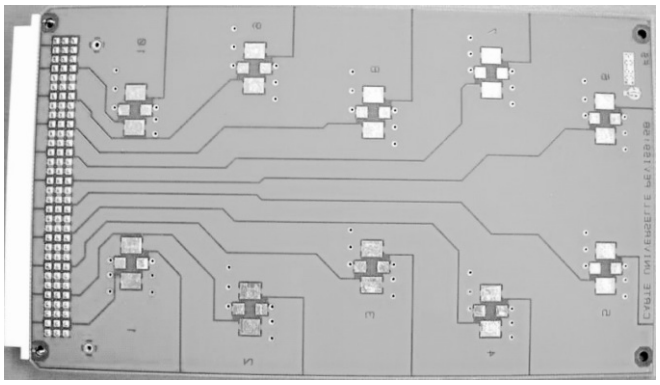
Picture 3
MCu PCB

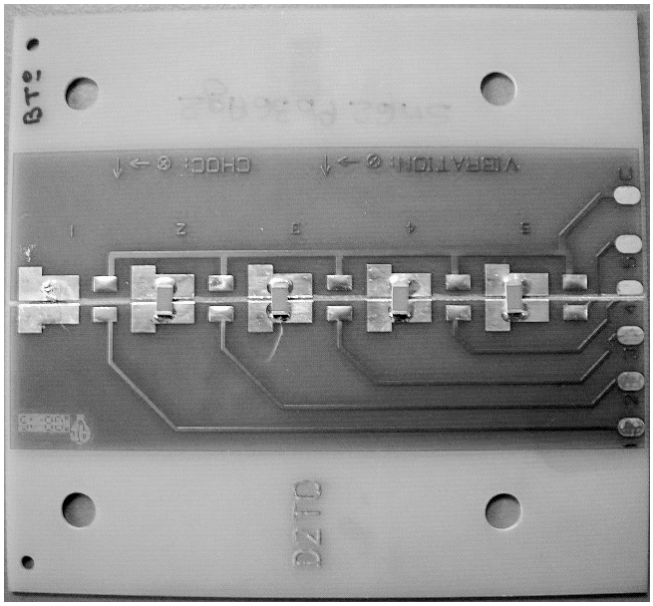
Front view



Rear view



Picture 4
Heat sink PCB
enlarged terminations



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