



Thin Film Single Value Chip and Wire Capacitors



Product may not be to scale

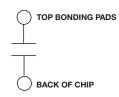
The NC series of thin film capacitors has the advantage of increased performance and smaller size when compared with its thick film counterparts. These chips are available in sizes down to 20 mil square and in capacitances up to 1000 pF.

Parts require epoxy or eutectic die attach to substrate and one wire bond.

These chips are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The NC's are 100 % electrically tested and visually inspected to MIL-STD-883.

ELECTRICAL SCHEMATIC NCAA, NCBB, NCCC





FEATURES

- Wire bondable
- Small size: 0.020 inches square to 0.060 inches square
- · Substrate: silicon with gold backing
- Dielectric: silicon dioxide / silicon nitride
- Capacitance range: 0.5 pF to 1000 pF
- · Material categorization: for definitions of compliance www.vishay.com/doc?99912



RoHS COMPLIANT

HALOGEN FREE **GREEN**

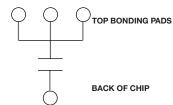
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APPLICATIONS

The NC series of capacitor chips are designed for assembly in hybrid circuits using conventional wire-bonding techniques. They provide excellent stability and performance, and their small size gives the hybrid designer greater layout flexibility. They are available as MNOS or MOS capacitors. The MOS version is to be preferred when low dielectric absorption is required.

ELECTRICAL SCHEMATIC NCDD, NCEE





WV (DC) VALUES AND TOLERANCES									
CAPACITOR MODEL	NCAA	NCBB	NCCC	NCDD	NCEE	UNIT			
Case Size	0202	0303	0404	0505	0606				
Capacitance Values	0.5 to 51	33 to 100	56 to 220	150 to 510	360 to 1000	pF			
Tolerance	± 2.5, ± 5, ± 10, ± 20, ± 25	± 2.5, ± 5, ± 10, ± 20	%						
DC Working Voltage	200	150	190	140	See section "DC Working Voltages and Tolerances"	V			

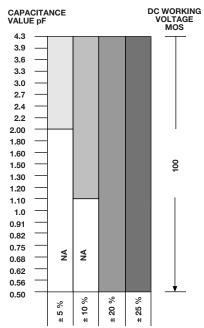
STANDARD ELECTRICAL SPECIFICATIONS					
PARAMETER	VALUE	UNIT			
Capacitance Range	0.5 to 1000	pF			
Maximum Working Voltage	200	V			
Peak Voltage at +25 °C	1.5 x working voltage				
Dissipation Factor, 1 kHz, 1 V _{RMS} , +25 °C	0.05 MNOS 0.1 MOS	%			
Q at 1 mHz, 50 mV _{RMS} , +25 °C	1000 min.				
TCC, -55 °C to +150 °C	+45 ± 25 MNOS +15 ± 25 MOS	ppm/°C			
Insulation Resistance at Working Voltage, +25 °C	10 ⁹ min.	Ω			
Operating Temperature Range	-55 to +125	°C			
Thermal Shock	± 0.25 + 0.25 pF max. ∆C/C	%			
Moisture Resistance, MIL-STD-202, Method 106	± 1.0 + 0.25 pF max. ΔC/C	%			
Short Time Overload, +25 °C, 5 s, 1.5 x Working Voltage	± 0.25 + 0.25 pF max.	%			
High Temperature Exposure, 100 h at 150 °C Ambient	± 0.25 + 0.25 pF max. ΔC/C	%			
Life, MIL-STD-202, Method 108 Condition D, +125 °C Ambient, 1000 h at Working Voltage	± 0.25 + 0.25 pF max. ΔC/C	%			

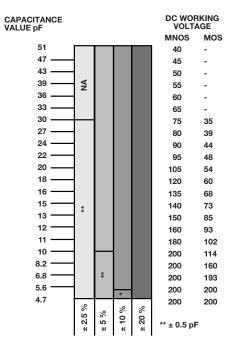
Revision: 20-Mar-2023 Document Number: 61033



DC WORKING VOLTAGES VALUES AND TOLERANCES

NCAA 0.020 inches square



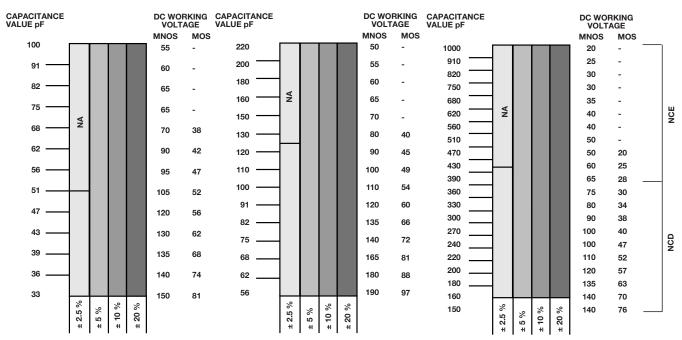


NA = NOT AVAILABLE

NCBB 0.030 inches square

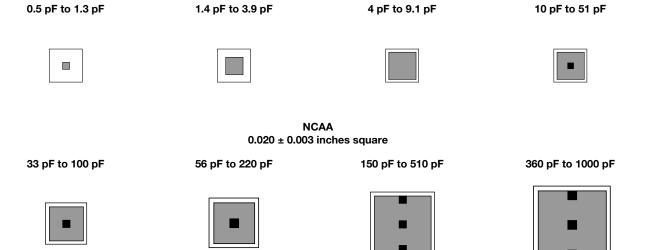
NCCC 0.040 inches square

NCEE 0.060 inches square NCDD 0.055 inches square



Vishay Electro-Films

DIMENSIONS



NCBB 0.030 ± 0.003 inches square NCCC 0.040 ± 0.003 inches square

 $\begin{array}{c} \text{NCDD} \\ \text{0.055} \pm \text{0.003} \text{ inches square} \end{array}$

NCEE

NCEE 0.060 ± 0.003 inches square

Note

 Due to VEFI standard trim-etch process, exposed dielectric may be observed. This feature shall not be considered metal mis-alignment and is deemed acceptable

MECHANICAL SPECIFICATIONS				
PARAMETER	VALUE			
Chip Size	Per diagrams			
Chip Thickness	0.010" ± 0.002" (0.25 mm ± 0.05 mm)			
Chip Substrate Material	Semiconductor silicon			
Dielectric	Silicon dioxide/silicon nitride			
Bond Pad	0.005" x 0.005" min., 10 kÅ aluminum			
Backing	3 kÅ min. gold			

Options: gold bond pads 15 kÅ; lower profile version is available, consult applications engineer

GLOBA	GLOBAL PART NUMBER INFORMATION								
	SAP Part Number: NCAA4700CKMAHWS NCEE10000KNGKWS NCEE10000KNGKWS NCEE10000KNGKWS								
SAP Desi	SAP Description: NCAA 4.7 pF 10 % MOS AI H WS NCEE 1000 pF 10 % MNOS Au K WS								
	N C A A	4 7	0 0	СК	MA	H W	S		
						玉 一			
MODEL	CAPACITANCE MU	ACITANCE JLTIPLIER CODE	OLERANCE CODE	DIELECTRIC	TERMINATION	VISUAL CLASS	PACKAGING CODE		
NCAA	First 4 digits D :	= 0.0001 D	$= \pm 0.5 pF$	$\mathbf{M} = MOS$	G = Au	H = class H	WS =		
NCBB	are significant C	= 0.001 F	H = 2.5 %	N = MNOS	$\mathbf{A} = AI$	K = class K	waffle pack		
NCCC	figures of B	3 = 0.01	J = 5.0 %			<u> </u>	100 min.,		
NCDD	capacitance	A = 0.1	K = 10 %				1 mult.		
NCEE		0 = 1	M = 20 %						
	. "								



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Vishay

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