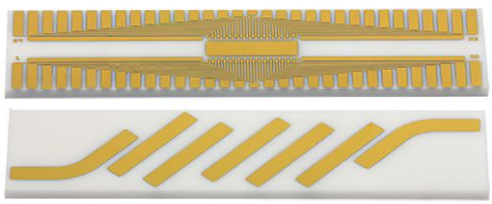
Custom Substrates - Conductor Pattern



FEATURES

- Precision conductor patterns
- Metalization on 1 or 2 surfaces
- Various substrate materials
- Sputtered / plated metal systems
- Custom sizes from 0.020" x 0.020" to 4.000" x 4.000"
- Quick delivery available

APPLICATIONS

Vishay EFI custom specialty films / conductor patterned substrates are used in the hybrid circuit and microwave industries. These conductor patterns are precisely manufactured to be used for complex fan-outs, interconnects, high temperature, and RF / microwave designs. Vishay EFI custom specialty films / conductor patterned substrates can also be used in a wider variety of applications including jumpers, mounting pads, and bonding pads. The custom specialty film / conductor patterned substrates are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The custom specialty film / conductor patterned substrates are visually inspected to MIL-STD-883, method 2032 class H or K.

THIN FILM DESIGN GUIDELINES

Thin Film Design Guide for RF and UWave Substrates (www.vishay.com/doc?49109).

SUBSTRATE MATERIALS

For substrate materials and their properties, please reference datasheet: SPF1 (www.vishay.com/ppg?61105).

DEFINING A METAL SYSTEM

Vishay EFI offers several different metals to meet the custom needs of our customers. Simple conductor circuits have the most flexibility with available metal systems. As the complexity and level of integration increase, the list of available metal system choices is limited to allow for tighter process control and manufacturability. The following table identifies the specific function of the available metals as well as their available thickness ranges.

AVAILABLE METALS AND THEIR FUNCTIONS			
LAYER TYPE	METAL	RANGE OF VALUES	COMMENTS
Adhesion	Titanium tungsten (TiW)	500 Å to 1250 Å	Ideal for high temperatures
	Chromium (Cr)	500 Å to 1250 Å	Ideal for low temperatures
Barrier	Nickel (Ni)	1250 Å to 1750 Å	Sputtered barrier
	Palladium (Pd)	1500 Å to 2500 Å	High temperature solder barrier
Conductor	Gold (Au)	10 μ" to 200 μ" (0.25 μm to 5 μm)	-
	Copper (Cu)	20 μ" to 200 μ" (0.05 μm to 5 μm)	-
	Aluminum (Al)	50 μ" to 120 μ" (1.27 μm to 5 μm)	Aluminum wire bond
High Current Conductor	Gold (Au)	200 μ" to 1000 μ" (5 μm to 25 μm)	Gold wire bond
	Copper (Cu)	200 μ" to 4000 μ" (5 μm to 100 μm)	High temperature / conductivity

Note

- TaN and NiCr are available as adhesion metal layers under certain metal stacks. Call factory for details

APPLICATION OF METAL SYSTEMS

A metal system should be selected based upon electrical, thermal, and mechanical performance demands as well as the assembly process requirements. Assembly requirements might include pads suitable for eutectic (solder) bonding and / or wire bonding.

Soldering pads should include a barrier layer designed to control the solubility of the pad metallization with the solder being applied. A nickel or palladium barrier layer is typically deposited under gold soldering pads to ensure reliable device attachment due to gold's high solubility in solders.

All of the standard metal systems offered by Vishay EFI are readily bonded using gold wire. For optimal bond integrity, a minimum of 100 μ" (2.5 μm) gold thickness is recommended, although reasonable bonding results can be achieved with gold as thin as 50 μ" (1.2 μm).

Intermetallic formation and barrier metal migration are influenced by film exposure to high temperatures. For this reason, it is important to select a metal system that can withstand the temperature profile requirements of the application. The following table provides a matrix of standard metal systems and assembly options.

STANDARD METAL SYSTEMS AND ASSEMBLY OPTIONS

METAL SYSTEM	MAX. REFLOW TEMPERATURE	WIRE-BONDABLE GOLD	SOLDER TYPE	
			LEAD / LEAD (Pb)-FREE	GOLD BEARING
Cr / Cu / Ni / Au	350	Yes	Preferred	Yes
NiCr / TiW / Au	400	Yes	-	Yes
NiCr / Ni / Au	350	Yes	Preferred	Yes
NiCr / TiW / Au / Ni / Au	350	Yes	Preferred	Yes
TiW / Au	450	Yes	-	Yes
TiW / Ni / Au	350	Yes	Preferred	Yes
TiW / Au / Ni / Au	350	Yes	Preferred	Yes
TiW / Pd / Au	450	Yes	Yes	Preferred
TiW / Au / Cu / Ni / Au	350	Yes	Preferred	Yes
TaN / TiW / Au	450	Yes	-	Yes
TaN / TiW / Ni / Au	350	Yes	Preferred	Yes
TaN / TiW / Au / Ni / Au	350	Yes	Preferred	Yes
TaN / TiW / Pd / Au	450	Yes	Yes	Preferred
TaN / TiW / Au / Cu / Ni / Au	350	Yes	Preferred	Yes

Additional metal system capabilities are available. These options are subject to review by the Vishay EFI engineering and production teams. Consideration will be given to special requests, with a focus on manufacturability and reliability.

INCORPORATING HIGH CONDUCTIVITY TRACES

Vishay EFI's capability to deposit thick conductor traces has enabled design approaches that allow high current, low resistance circuit traces to co-exist with microwave structures and transmission lines. For circuit traces carrying high currents over long distances, the resistive losses of thin film conductor lines can become significant. By selectively increasing the thickness of high-current lines, the engineer can have fine line RF structures on the same circuit with low-loss DC lines. Additionally, these low-resistance traces can be used to manage thermal loads within RF circuits.

Typically, the design engineer will calculate the trace resistance (R_{total}) of a structure during the design process. The trace resistance is defined as:

R_{total} = (trace length / trace width) x conductor sheet resistance
R_{total} = (L / W) x R_{sheet}.

The sheet resistance (R_{sheet}) is derived by dividing the bulk resistivity by the conductor thickness. Therefore, the thicker one can deposit the conductor, the lower the overall sheet resistance. The following two tables detail the bulk resistivity and the typical sheet resistance of some common thin film metals at a variety of deposition thicknesses.

SELECTED BULK RESISTIVITY		
MATERIAL	**THEORETICAL BULK RESISTIVITY μΩ x cm**	**CONSERVATIVE VALUE OF BULK RESISTIVITY WHEN DEPOSITED μΩ x cm**
Gold (Au)	2.2	2.4 (sputtered) / 2.9 (plated)
Titanium Tungsten (TiW)	-	45 (sputtered)
Copper (Cu)	1.71	2 (sputtered) / 4 (plated)
Nickel (Ni)	7	8.2 (sputtered)
Aluminum (Al)	2.7	3 (sputtered)

SELECTED APPROXIMATE SHEET RESISTIVITIES		
METAL	**THICKNESS μ" (μm)**	**PLATED SHEET RESISTIVITY (mΩ /sq)**
Gold (Au)	80 (2)	14.5
Gold (Au)	160 (4)	7.25
Gold (Au)	400 (10)	2.9
Copper (Cu)	1000 (25)	0.42
Copper (Cu)	2000 (50)	0.21
Nickel (Ni)	200 (5)	160 (sputtered)
Aluminum (Al)	40 (1)	30 (sputtered)

In summary, gold (Au) and copper (Cu) can be deposited at much greater thicknesses than standard thin films to reduce overall conductor resistance. Gold (Au) can be deposited up to a maximum thickness of 400 μ", while copper (Cu) can be plated routinely at thicknesses up to 4000 μ" (100 μm). It is important to note that minimum line widths and spaces increase with film thickness. See the following for a summary of line widths and spaces as associated with conductor thickness.

PATTERNING LINES AND SPACES

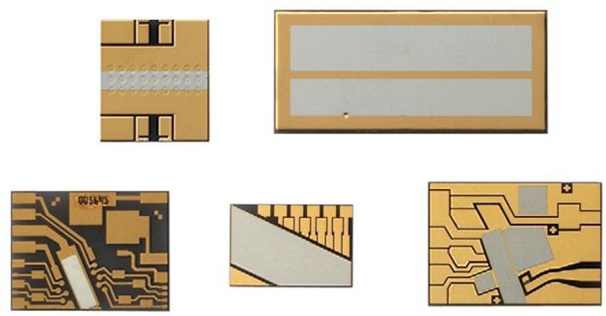
Thin film patterning tolerances are influenced by several factors in the photomasking process. Pattern tolerancing for plating and etching processes vary based on the metal thickness as shown in the tables below. As the thickness of the metal increases, the photoresist used for this process changes and the metal thickness tolerances and line and space patterning must be adjusted to compensate for this. As these decisions are made the surface finish of the substrate must also be factored as the polished surface finish will deliver the smoothest surface and therefore the best line and space pattern. For the substrate materials where As fired and lapped options are available these surfaces will not hold the same tolerances and minimum sizes that the polished surface will.

PLATED METAL PATTERNS			
TOTAL MAX. METAL THICKNESS	**BEST PATTERN TOLERANCE PROCESS**	**BEST PLATING THICKNESS TOLERANCE**	**SMALLEST PATTERN LINE AND SPACE**
100 μ" (2.54 μm)	± 0.1 mil	± 30 μ"	0.5 mil / 0.5 mil
150 μ" (3.8 μm)	± 0.15 mil	± 40 μ"	0.5 mil / 0.5 mil
250 μ" (6.35 μm)	± 0.2 mil	± 50 μ"	0.5 mil / 0.5 mil
400 μ" (10.2 μm)	± 0.2 mil	± 100 μ"	0.5 mil / 0.5 mil
800 μ" (20.3 μm)	0.3 mil±	± 150 μ"	1 mil / 1 mil
1000 μ" (25.4 μm)	± 1.0 mil	± 250 μ"	2 mil / 2 mil
2000 μ" (51 μm)	± 2.0 mil	± 500 μ"	3 mil / 3 mil
4000 μ" (102 μm)	± 3.0 mil	± 1 mil	5 mil / 5 mil

ETCHED METAL PATTERNS				
TOTAL MAX. METAL THICKNESS	BEST PATTERN TOLERANCE PROCESS	BEST METAL THICKNESS TOLERANCE	SMALLEST PATTERN LINE AND SPACE	METAL DEPOSITION
100 µ" (2.54 µm)	± 0.1 mil	Ref. plating table	1 mil / 1 mil	Plated
150 µ" (3.8 µm)	± 0.2 mil	Ref. plating table	1.5 mil / 1.5 mil	Plated
200 µ" (5.1 µm)	± 0.3 mil	Ref. plating table	2 mil / 2 mil	Plated
300 µ" (7.6 µm)	± 0.5 mil	Ref. plating table	2 mil / 2 mil	Plated
12 000 Å	± 0.5 mil	±10 %	1.5 mil / 2 mil	Sputtered
25 000 Å	± 1.0 mil	±10 %	2 mil / 2 mil	Sputtered

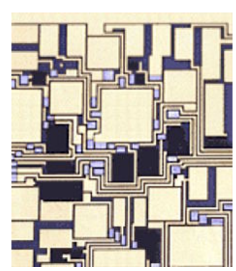
AuSn APPLICATIONS

Vishay EFI offers the option of a sputter deposition of gold-tin solder with wt % of 80 / 20 while maintaining tolerances tighter than ± 2 % wt and control of film thickness to ± 1.0 µm. This capability allows deposition of customer AuSn patterns that can be used to fine-tune assembly processes to meet the most demanding requirements; the tight composition tolerance eliminates the need to adjust reflow process parameters to compensate for variations in solder composition. The gold-tin deposition process allows films with thickness ranging between 4.5 µm and 7 µm with a tolerance of ± 1.0 µm. Common applications for AuSn deposition are laser diode sub-mounts, fiber optic pump lasers, optical transmitters, optical receivers, optical transceivers and optical TOSA / ROSA packages. For further detail, please reference document: AuSn design guideline (www.vishay.com/doc?49248).



HIGH TEMPERATURE APPLICATIONS

When designing hybrid assemblies to operate at temperatures above 125 °C it becomes important to provide monometallic interconnects to prevent intermetallic diffusion and resultant long term reliability problems. For these situations, Vishay Electro-Films (EFI) has developed processes for depositing both aluminum and gold bonding pads on the same substrate. This structure provides for monometallic interconnects. Aluminum wire can be used to connect from the aluminum pads on the substrate. Similarly, gold wire can be used to connect gold pads on the substrate to gold hermetic package terminals. Appropriate barrier metals are included in substrate processing to provide long term reliability in high temperature applications.



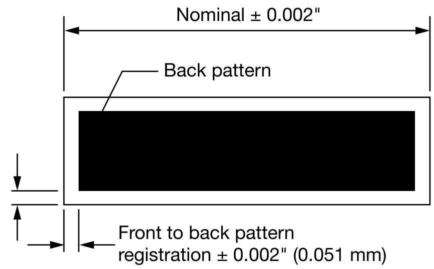
High temperature - Au and Al wirebond pads

SUBSTRATE SINGULATION

Vishay Electro-Films uses standard semiconductor / ceramic dicing equipment and processes to singulate production boards into individual pieces. These processes depend on tight alignment and inspection to maintain overall part dimension tolerances and metal pattern to part edge tolerances. Each of these dimensions and their tolerances are measured on each lot that is processed.

SUBSTRATE SINGULATION

DIMENSION	DIMENSION MEASUREMENT in inches (mm)	MINIMUM TOLERANCE in inches (mm)
Metal pattern pullback from edge of die	0.002 (0.0508)	± 0.002 (± 0.0508)
Overall part dimension	n/a	± 0.002 (± 0.0508)
Front to back pattern tolerance	n/a	± 0.002 (± 0.0508)



GLOBAL PART NUMBER INFORMATION

Custom Global Part Number: SPF2 05687 - 00 C

Custom Global Part Number Description: Specialty Films Custom 205687-00C

S	P	F	2	0	5	6	8	7	-	0	0	C
MODEL				CUSTOM PART NUMBER						INTERNAL REVISION		VARIANT

VARIANT:
A = AlN
B = BeO
C = conductor
F = ferrite/ garnet
K = zirconia

CONTACT INFORMATION

For design assistance, contact: efi@vishay.com

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