## SPICE Device Model SQ1431EH



Vishay Siliconix

## P-Channel 30 V (D-S) 175 °C MOSFET

### DESCRIPTION

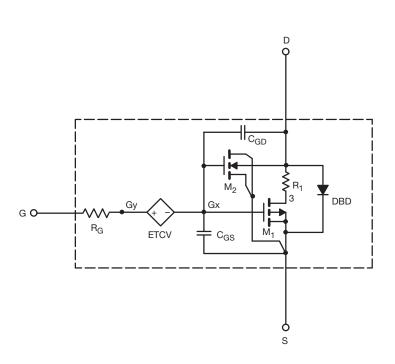
The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### **CHARACTERISTICS**

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

### SUBCIRCUIT MODEL SCHEMATIC



#### Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

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| <b>SPECIFICATIONS</b> (T <sub>J</sub> = 25 °C, unless otherwise noted) |                     |                                                            |                   |                  |      |
|------------------------------------------------------------------------|---------------------|------------------------------------------------------------|-------------------|------------------|------|
| PARAMETER                                                              | SYMBOL              | TEST CONDITIONS                                            | SIMULATED<br>DATA | MEASURED<br>DATA | UNIT |
| Static                                                                 |                     |                                                            |                   |                  |      |
| Gate Threshold Voltage                                                 | V <sub>GS(th)</sub> | $V_{DS} = V_{GS}$ , $I_D = -250 \ \mu A$                   | 1.7               | -                | V    |
| Drain-Source On-State Resistance <sup>a</sup>                          | R <sub>DS(on)</sub> | V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 2 A           | 0.126             | 0.125            | Ω    |
|                                                                        |                     | V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 1.6 A        | 0.240             | 0.230            |      |
| Forward Transconductance <sup>a</sup>                                  | <b>g</b> fs         | V <sub>DS</sub> = - 10 V, I <sub>D</sub> = - 2 A           | 3                 | 3                | S    |
| Diode Forward Voltage                                                  | V <sub>SD</sub>     | I <sub>S</sub> = - 1.2 A                                   | - 0.85            | - 0.85           | V    |
| Dynamic <sup>b</sup>                                                   |                     | ·                                                          |                   |                  |      |
| Input Capacitance                                                      | C <sub>iss</sub>    | V <sub>DS</sub> = - 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz | 167               | 164              | pF   |
| Output Capacitance                                                     | C <sub>oss</sub>    |                                                            | 42                | 44               |      |
| Reverse Transfer Capacitance                                           | C <sub>rss</sub>    |                                                            | 29                | 28               |      |
| Total Gate Charge                                                      | Qg                  | $V_{DS}$ = - 15 V, $V_{GS}$ = - 10 V, $I_D$ = - 2.2 A      | 3.4               | 4.2              | nC   |
| Gate-Source Charge                                                     | Q <sub>gs</sub>     |                                                            | 0.70              | 0.70             |      |
| Gate-Drain Charge                                                      | Q <sub>gd</sub>     |                                                            | 1                 | 1                |      |

Notes

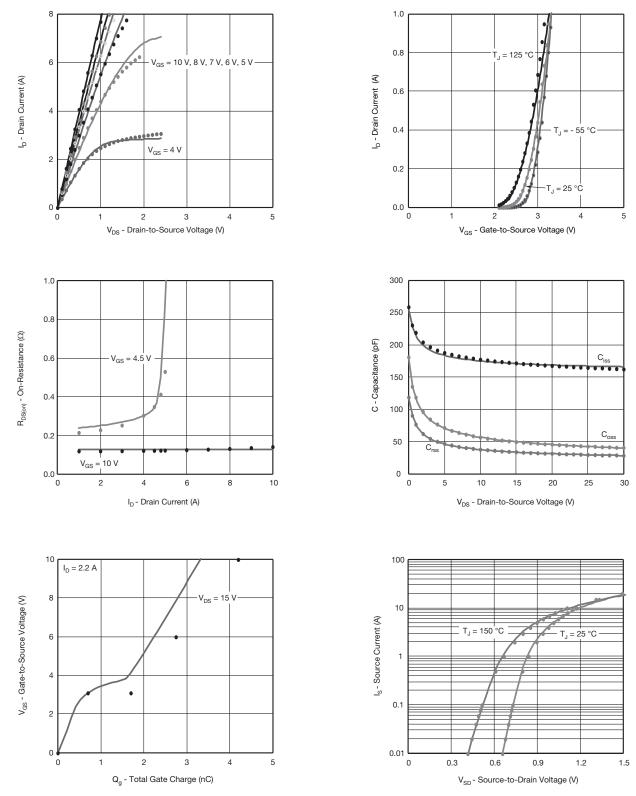
a. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%.$ 

b. Guaranteed by design, not subject to production testing.



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### COMPARISON OF MODEL WITH MEASURED DATA (T<sub>J</sub> = 25 °C, unless otherwise noted)



#### Note

• Dots and squares represent measured data.

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