18 V, 60 A, 0.6 mΩ $R_{DS(on)}$ Hot-Swap eFuse Switch

DESCRIPTION

The SiC32301, SiC32302, SiC32303, and SiC32304 are programmable hot swap e-fuses for high current applications such as servers, data storage, and communication products. They contain a high side MOSFET and control circuitry that enables them to work as stand-alone devices, or to be controlled by a hot-swap controller. The SiC32301, SiC32302, SiC32303, and SiC32304 drive up to 60 A of continuous current per device.

The SiC32301, SiC32302, SiC32303, and SiC32304 limit the inrush current to the load when a circuit card is inserted into a live backplane power source, thereby limiting the backplane's voltage drop.

The devices offer many features to simplify system designs. They provide an integrated solution for monitoring output current and die temperature, eliminating the need for an external current sensing shunt resistor, power MOSFET, and thermal sensing device.

The SiC32301, SiC32302, SiC32303, and SiC32304 detect the power FET gate, source, and drain short conditions, in addition to feedback to the controller. Also, the SiC32301 and SiC32303 can be operated in parallel for higher current applications. The SiC32301, SiC32302, SiC32303, and SiC32304 are available in a 5 mm x 5 mm QFN package.

FEATURES

- 4.5 V to 18 V operating input range
- 25 V guaranteed maximum input tolerance
- Maximum 60 A output current
- Integrated switch with lower $R_{DS(on)}$ 0.6 mΩ
- Built-in MOSFET driver
- Integrated current sensing with sense output
- Separate current sensing output used to program over-current value
- Built-in soft start and insertion delay
- Output short-circuit protection
- Over-temperature protection
- Built-in fuse health diagnostics
- Fault and power good signal outputs
- Parallel operation for higher current applications, SiC32301 and SiC32303 only
- Analog temperature report
- Output voltage power down control
- Available in a FCQFN 5 mm x 5 mm package

APPLICATIONS

- Hot swap
- PC cards
- Disk drives
- Servers
- Networking

TYPICAL APPLICATION CIRCUIT

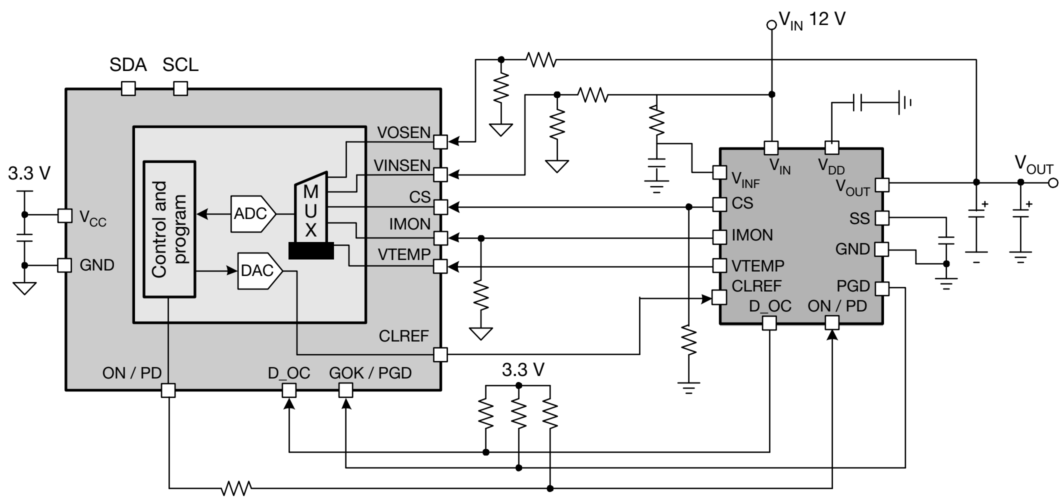


Fig. 1 - Typical Application Circuit

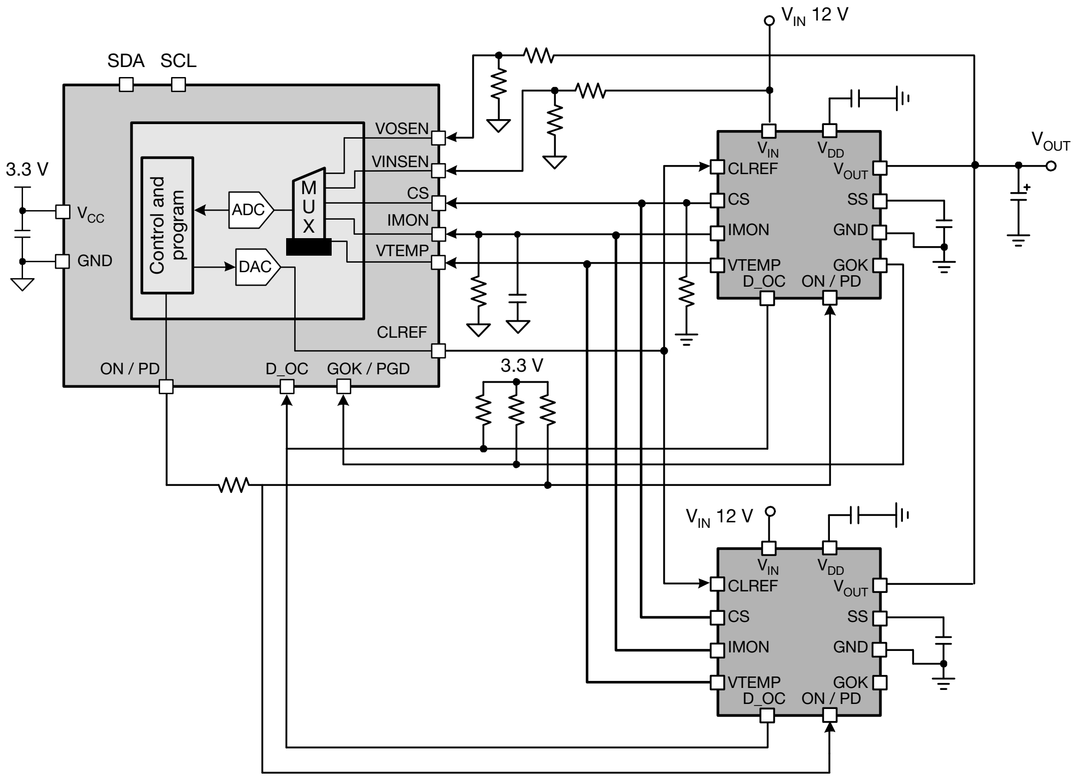


Fig. 2 - SiC3230x Typical Application Diagram

PINOUT CONFIGURATION

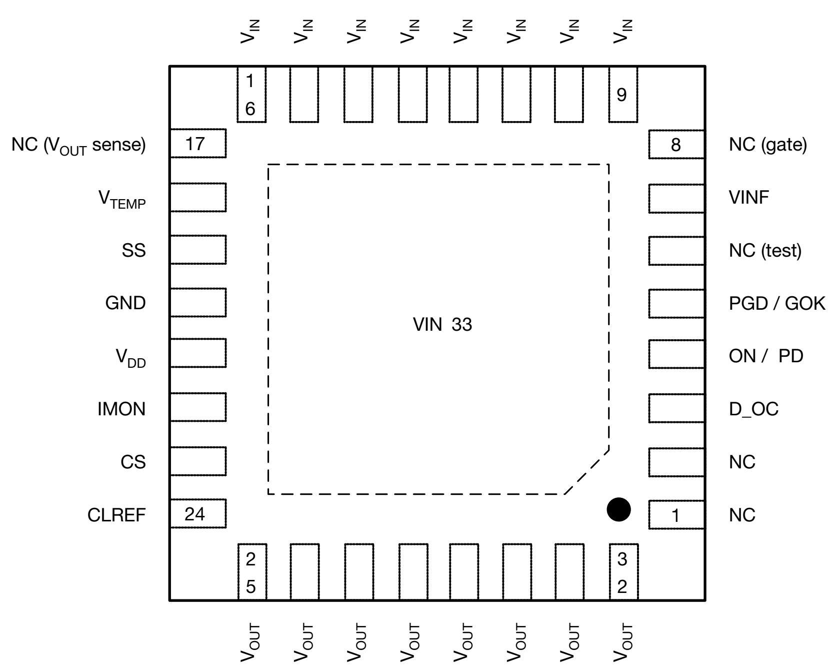


Fig. 3 - Pins Out Configuration (Top View)

ORDERING INFORMATION

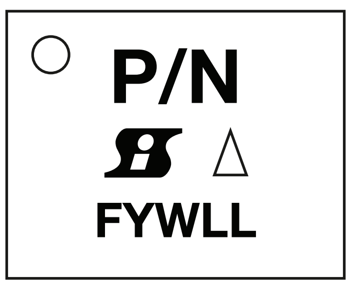
PART NUMBER	PACKAGE	FAULT RESPONSE	ALERT PINS	MARKING CODE
SiC32301CD-T1E3	PowerPAK MLP55-32	Switch off, and latch upon fault event	PGD, D_OC	32301
SiC32301CD-T5E3				
SiC32302CD-T1E3		Auto-retry, 1s after fault is removed		32302
SiC32302CD-T5E3				
SiC32303CD-T1E3		Switch off, and latch upon fault event	GOK, D_OC	32303
SiC32303CD-T5E3				
SiC32304CD-T1E3		Auto-retry, 1s after fault is removed		32304
SiC32304CD-T5E3				
SiC32301EVB	Reference board			
SiC32302EVB				
SiC32303EVB				
SiC32304EVB				

PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 2	NC	May connect to GND, V_{OUT}, or left floating
3	D_OC	Digital output of over-current indication. D_OC is an open-drain output. When the voltage on CS is higher than 85 % x VCLREF, D_OC logic is pulled low. This pin has an internal 2 μA pull-down current to artificially pull low in case the external pull-up resistor is missing
4	ON / PD	Power FET on / off control or OUT voltage pull-down mode control. Drive ON / PD higher than 1.4 V to turn on the power FET after setting ON / PD equal to 1.1 V for 2 ms will cause the controller to recognize a V_{OUT} discharge request. The power FET will begin to discharge with a 500 Ω internal resistor. Drive ON / PD below 0.8 V to open the power FET. In the event of a latching fault or inadequate input V_{IN} supply, a 1 MΩ resistor will attempt to discharge the ON / PD pin (useful for stand-alone applications). Do NOT float ON / PD
5 (SiC32301, SiC32302)	PGD	Digital output of power good indication. At initial stage, PGD is set to low by an open drain output. When V_{OUT} reaches 98 % of V_{IN}, PGD pin will turn high. There is a 5 % hysteresis. PGD is hold low at soft start stage. If a fault is detected, PGD will not be asserted or will be deserted. This pin has an internal 2 μA pull-up current to artificially pull the signal high in case the external pull- up resistor is missing. The PGD flags on the faults of T_J over temperature, switch health check failure, severe over current, CS voltage is higher than CLREAF voltage for 250 μs, 200 ms soft-start timer expires / soft start failure. A fault of any paralleled part should pull the common PGD node low under parallel configuration operation when PGDs are connected together
5 (SiC32303, SiC32304)	GOK	If a fault is detected, GOK will pull low, and the switch is turn off. If the fault is caused by an OVER-CURRENT event, OVER-TEMPERATURE event or OVER-POWER event, then the GOK will latch. Other faults monitored which do not cause a latch unless the 200 ms soft-start timer expires are DRAIN-SHORT short, GATE-SOURCE short, GATE-DRAIN short, and SOFT-START FAIL. The OVER-CURRENT event will cause a GOK latch immediately if the current is greater than 100 A or if the CS voltage is greater than the CLREF voltage for 250 μs. Power or ON / PD cycling is required if the GOK latches. FET health is monitored at startup via DRAIN / GATE / SOURCE short detection but does not latch GOK unless 200 ms timer expires. This pin has an internal 2 μA pull-down current to artificially pull the signal low in case the external pull-up resistor is missing
6	NC (TEST)	Do not connect to this pin; leave floating
7	V_{INF}	This pin is an optional filtered V_{IN} pin. Connect an appropriate RC filter to filter noise on V_{IN}
8	NC (Sense)	Do not connect to this pin; leave floating
9 to 16	V_{IN}	System input power supply. The SIC32301 operates from a +4.5 V to +16 V input rail.
17	NC	No internal connection

PIN DESCRIPTION		
PIN	**NAME**	**FUNCTION**
18	V_{TEMP}	Junction temperature sense output. The output temperature equals 400 mV + 10 mV/°C x T_J
19	SS	The SS pin is the ramping control for soft-start ramping rate. An internal fixed current source charges an external capacitor in linear fashion. The V_{OUT} voltage soft-starts at a rate that tracks the soft-start capacitor. If soft-start has not completed within 200 ms, a fault is declared. In the event that the soft- start ramp is too fast and causes in-rush current to charge V_{OUT} with too much current, the CLREF reference will override (slow down) the soft-start ramp rate. The ramping voltage on the SS pin will equal 10 % of the V_{OUT} voltage during ramping
20	GND	Signal ground
21	V_{DD}	Internal 5 V LDO output. Place a 1 μF decoupling capacitor close to V_{DD} and GND
22	I_{MON}	Current monitor output. The output current is proportional to the current flowing through the power device. The I_{MON}/I_{OUT} gain is 10 μA/A with 5 μA off set
23	CS	Current sense output. CS requires an external resistor. The V_{CS} voltage is compared with CLREF to determine the current limit
24	CLREF	Current limit reference voltage input. An internal 10 μA current is sourced from this pin to an external resistor. During soft-start, this current is further internally limited such that the developed external voltage is not more than 200 mV until V_{OUT}/V_{IN} > 30 %, 600 mV (approximately) until V_{OUT}/V_{IN} > 80 %, and 1.6 V once > 80 %. This pin can be manually controlled / driven by an external DAC that can overdrive 10 μA. The 600 mV threshold actually tracks an internal diode voltage and decreases with increasing temperature
25 to 32	V_{OUT}	Output voltage controlled by the IC. OUT is connected to the source of the integrated MOSFET
33	V_{IN}	Input of hot swap power switch

MARKING CODE



Format:

- Line 1: part number
- Line 2: Siliconix logo and ESD logo
- Line 3: factory code, year code, work week code, lot code

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	**SYMBOL**	**MIN.**	**MAX.**	**UNIT**
Input voltage, output voltage	V_{IN}, V_{OUT}, V_{INF}	-0.3	+25	V
Internal 5 V LDO output	V_{DD}	-0.3	-0.3 to +6	V
All other pins		-0.3	-0.3 to V_{DD} + 0.3	V
Operating junction temperature range	T_J	-40	+150	°C
Lead temperature	T_{SLD}	-	260	°C
Storage temperature	T_{STG}	-65	+150	°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE				
PARAMETER	MIN.	TYP.	MAX.	UNIT
Input voltage (V_{IN})	4.5	-	18	V
Maximum continuous output current	-	-	60	A
Maximum peak output current	-	-	80	A
V_{DD} output capacitance range	2.2	-	10	μF
CLREF voltage range	0.2	-	1.6	V
Operation junction temperature	-40	-	+125	°C

SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS SPECIFIED V_{IN} = V_{INF} = 12 V, ON / PD = 3.3 V, CVINF = 0.1 μF, CVDSS = 4 μF, CVTEMP = 0.1 μF, RVTEMP = 1 kΩ, CSS = 100 nF, min. / max. limits are over the junction temperature range of -40 °C to + 125 °C unless specified otherwise, typical values at T_A = 25 °C	LIMITS MIN.	TYP.	MAX.	UNIT
Supplies Current						
Quiescent current	I_Q	V_{ONPD} = 3 V, no load	-	3.15	-	mA
		Fault latch off	-	6.5	-	μA
		V_{ONPD} = 0 V	-	6.15	-	mA
V_{DD} Regulator and UVLO						
Regulator output voltage	V_{VDD}	I_{VDD} = 0 mA, V_{INF} = 6 V	-5%	5	5%	V
V_{DD} current limit		V_{IN} = V_{INF} = 6 V or 12 V	45	70	-	mA
V_{DD} drop out voltage		V_{INF} = V_{IN} = 4.5 V, I = 20 mA	-	155	200	mV
UVLO threshold, rising			-	4.2	-	V
UVLO threshold hysteresis			35	75	-	mV
V_{IN} Under Voltage and Over Voltage Protections						
V_{IN} under voltage lockout threshold rising	V_{VIN_THR}		8.55	9	9.45	V
V_{IN} under-voltage lockout hysteresis	V_{VIN_THF}		-	0.4	-	V
ON / PD						
Internal current source	I_{ON_PD}		3.8	4.2	4.6	μA
FET on insertion delay time	t_{ON_DLY}	**Note:** 1 ms timer begins after ON_PD pin transitions above 1.4 V	-	1	-	ms
FET on high-level input voltage	V_{ON_Hi}		1.25	1.35	1.45	V
FET on-state hysteresis	V_{ON_Hyst}		-	0.1	-	V
Switch off discharge upper threshold	V_{PD_Hi}	**Note:** ON / PD must be held continuously between the value of 0.8 V and 1.2 V for 80 μs before command to discharge is recognized. Discharging will commence 2 ms after command is recognized	-	1.2	-	V
Switch off discharge lower threshold	V_{PD_Lo}		-	0.8	-	V
PD mode pull-down resistor	R_{PL_DN}	Internal resistor from V_{OUT} to ground through PD controlled functionality	-	625	-	Ω
PD mode pull-down delay time	$t_{PL\_DN\_DLY}$	**Note:** This 2.08 ms is the summation of the 80 μs recognition time and 2 ms delay time	-	2.05	-	ms
ON / PD pull-down resistor	R_{PL_ONPD}	Discharge resistor on ON / PD pin activated while V_{IN} not ready	-	1	-	MΩ
Soft-Start						

SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS SPECIFIED $V_{IN} = V_{INF}$ = 12 V, ON / PD = 3.3 V, CVINF = 0.1 µF, CVDSS = 4 µF, CVTEMP = 0.1 µF, RVTEMP = 1 kΩ, CSS = 100 nF, min. / max. limits are over the junction temperature range of -40 °C to + 125 °C unless specified otherwise, typical values at T_A = 25 °C	LIMITS MIN.	TYP.	MAX.	UNIT
Pull-up current	I_{SS}	T_J = 25 °C	4.5	5.2	6	µA
Gain to V_{OUT}	AVSS	30 %	8.6	10.4	12.2	V/V
		60 %	9.35	10.3	11.25	V/V
		90 %	9.6	10.3	11	V/V
SS pulldown voltage	VOL_SS	0.1 mA into pin during ON delay	-	6.7	-	mV
GOK Output (SiC32303, SiC32304), PGD Output (SiC32301, SiC32302)						
Output low current capability	I_{PGD_ACTIVE}	V_{PGD} = 0.2 V	18	20	25	mA
GOK / PGD off-state leakage current	I_{GOK_LKG}	V_{PGD} = 5 V **Note:** There is an intentional internal 2 MΩ pull down resistor	-	2.7	-	µA
I_{MON}, Current Sense						
Sense gain			-	10	-	µA/A
Pre-bias offset current			-	5.2	-	µA
Current monitor accuracy	I_{MON_ACC}	0.5 A < I_{OUT} < 3 A, T_J = 0 °C to 85 °C	-20	-	+20	%
		3 A < I_{OUT} < 10 A, T_J = 25 °C	-3	-	+3	%
		3 A < I_{OUT} < 10 A, T_J = 0 °C to 85 °C	-5	-	+5	%
		10 A < I_{OUT} < 60 A, T_J = 25 °C	-2	-	+2	%
		10 A < I_{OUT} < 60 A, T_J = 0 °C to 85 °C	-4	-	+4	%
Gain accuracy		10 A ≤ I_{OUT} ≤ 60 A	-5	-	5	%
Over-current threshold for D_OC signal pulling down	V_{DOC_TH}		83	87	90	%
Short - Circuit Protection						
Short-circuit current trip point	I_{SC}	SiC32301, SiC32303	-	100	-	A
		SiC32302, SiC32304 (auto retry)	-	80	-	A
Response time	t_{SC}		-	200	-	ns
CLREF						
Internal current source	I_{CLREF}	T_J = 25 °C	9.5	10	10.5	µA
		-40 < T_J < 125 °C	8	-	12	uA
Internal max. current limit clamp at various V_{OUT} levels	V_{CLREF_CLMP}	T_J = 25 °C, V_{OUT} < 40 % V_{IN} (relevant for shorted output during startup)	120	150	185	mV
		T_J = 25 °C, 40 % V_{IN} < V_{OUT} < 80 % V_{IN}	435	495	555	mV
		V_{CLREF} > 1.6 V, V_{OUT} > 80 % V_{IN}	1.45	1.6	1.7	V
		T_J = 125 °C, 40 % < V_{OUT} < 80 % V_{IN}	435	495	555	V
Over-current regulation time	$t_{CL\_REG\_OC}$	During normal operation	200	250	300	µs
CLREF current source clamp voltage			-	4.5	-	V

Notes
- Typical limits are established by characterization and are not production tested
- Guaranteed by design
- Min. and Max. Parameters are not 100% production tested

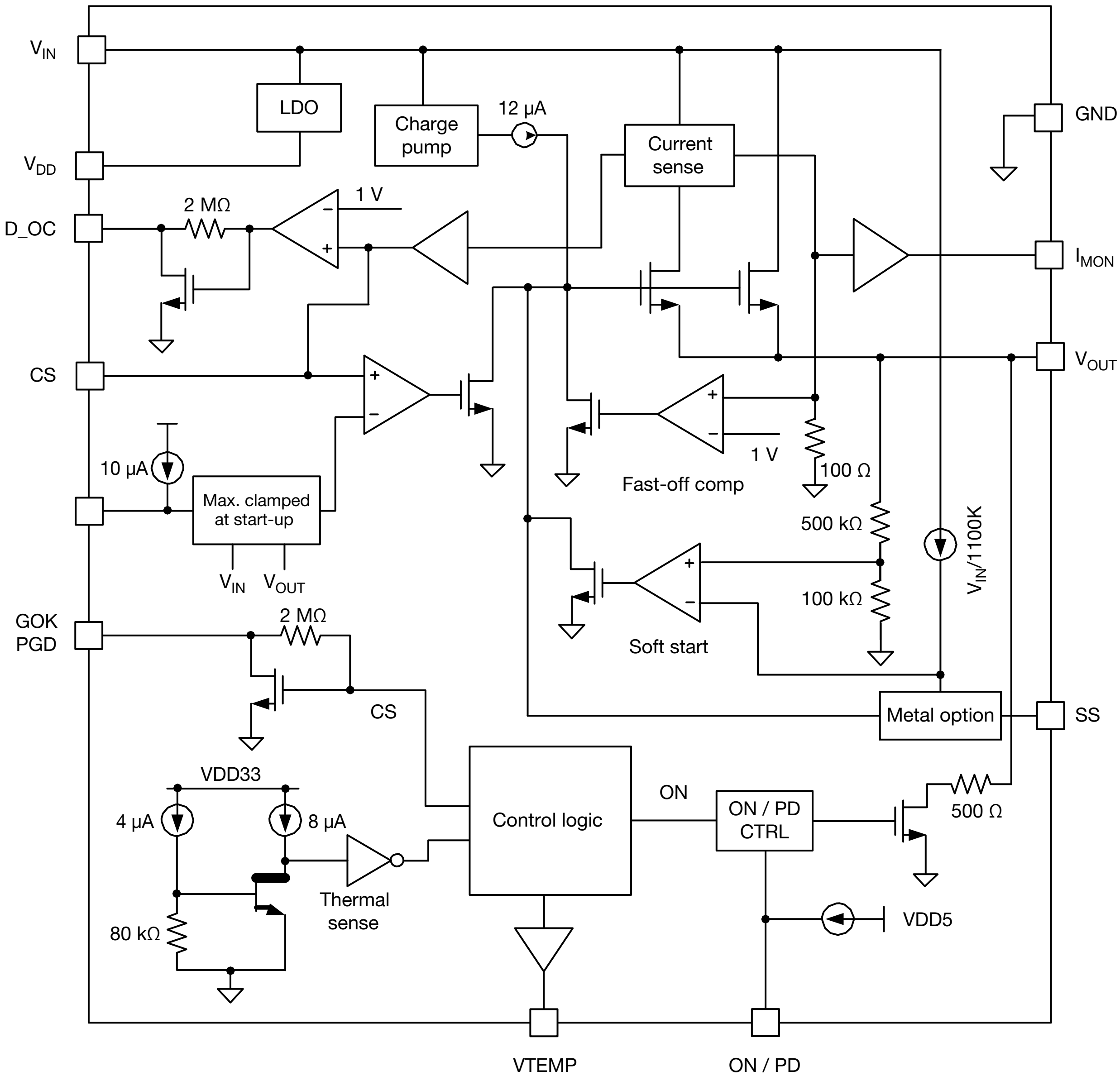
SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS SPECIFIED V_{IN} = 12 V, V_{DD}, = 5.0 V, T_A = 25 °C, unless otherwise noted	LIMITS MIN.	TYP.	MAX.	UNIT
D_OC Output						

SPECIFICATIONS						
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS SPECIFIED** V_{IN} = 12 V, V_{DD}, = 5.0 V, T_A = 25 °C, unless otherwise noted	**LIMITS**			**UNIT**
			MIN.	**TYP.**	**MAX.**	
D_OC pull down current	I_{DOC_ACTIVE}	V_{DOC} = 0.1 V	-	10	-	mA
D_OC bar off-state leakage current	I_{DOC_LKG}	**Note:** There is an intentional internal 2 MΩ pull down resistor	-	2.7	-	μA
D_OC flag response time		Load current cross from 80 % to 90 % in 1 μs, both rise and fall of VSC	-	1	5	μs
VTEMP						
Sense Gain		Sense range 0 °C to 140 °C	-	10	-	mV / ?
Sense Offset		V_{TEMP} = 450 mV + 10 mV/°C	410	450	490	mV
Pull down current		At 25 °C	-	50	-	μA
Thermal Shutdown						
Thermal shutdown temperature	T_{THDN}	GO/PGD pulls low	-	140	-	°C
Power MOSFET						
On resistance	$R_{DS(on)}$	T_J = 25 °C	-	0.6	1	mΩ
		T_J = 85 °C	-	0.7	-	mΩ
Off-state leakage current	I_{LKG_OFF}		-	-	40	mA
FET Health Diagnostic (Fault Detection)						
FET VDS short threshold	V_{SCTH_DS}	Startup postponed if V_{OUT} > V_{SCTH_DS} anytime after postponed **(Note: this is a non-latching fault)**	-	80	-	%
FET VDS short release threshold. (short flag removed threshold)	V_{DS_OK}	Startup resumed if V_{OUT} < V_{DS_OK} anytime after postponed	-	70	-	%
FET gate to drain short threshold	V_{SCTH_DG}	Startup postponed if V_G is less than V_{SCDG_TH} at V_{ON} > V_{ON_HI} transition. It will resume once it is below V_{DG_OK} **(Note: this is a non-latching fault)**	-	2.2	-	V
FET gate to drain short OK threshold	V_{DG_OK}	Startup resumed if V_G < V_{DG_OK} anytime after postponed	-	2	-	V
VG low threshold	V_{G_TH}	Restart / latch if V_{GD} < V_{G_TH} after t_{SS_MAX}. During normal operation, it will be a flag and triggers restart / latch	-	4	-	V
V_{OUT} low threshold	V_{OUTL_TH}		-	90	-	%
FET maximum gate fault timer	t_{gf_max}	After ON / PD goes high, if V_{GS} remains low for longer than 200 ms **(Note: this fault causes GOK to latch)**	-	200	-	ms
Maximum soft-start time	t_{SS_MAX}	After ON / PD goes high, if V_{OUT} < 90 % V_{IN} within 200 ms, or if V_{GS} remains less than 1.5 V below internal charge pump voltage (indication of fuse not fully on) within 200 ms **(Note: this fault causes GOK to latch)**	-	200	-	ms
Auto-Retry (SiC32302, SiC32304)						
Auto-retry delay	t_{DLY_RE}	Delay from power off / fault release to retry of startup	-	1	-	s

Notes

- Typical limits are established by characterization and are not production tested
- Guaranteed by design
- Min. and Max. Parameters are not 100% production tested

FUNCTIONAL BLOCK DIAGRAM



DETAILED OPERATIONAL DESCRIPTION

SIC3230 is a 60 A integrated high-side MOSFET with $R_{DS(on)}$ 0.6 mΩ, ideally suited for multi-fuse hot-swap applications. It works stand-alone or is controlled by a hot-swap controller for multi-fuse operation.

The SIC32301 limits the inrush current to the load when a circuit card is inserted into a live backplane power source, thereby limiting the backplane's voltage drop. It provides an integrated solution to monitor the output current and the die temperature, eliminating the need for an external current-sense power resistor, power MOSFET, and thermal sense device. Also, it provides monitored current and temperature information feedback to the processor or controller. The SIC32301 limits the internal MOSFET current by controlling the gate voltage through the current limit reference input and soft start ramp.

Power-Up Sequence

For hot-swap applications, the input of the SiC32301 can experience a voltage spike or transient during the hot-plug procedure. This is caused by the parasitic inductance of the input trace and the input capacitor. A fixed 1 ms insertion delay stabilizes the input voltage.

If the SIC32301 is controlled by a front-end hot- swap controller, there will be a time-on delay before ON / PD can turn on the power FET. This stabilizes the input voltage when GOK becomes high.

As shown in Fig. 4, the input voltage rises immediately. The power FET GATE voltage should always be pulled low during the V_{IN} plug-in with high dV/dt. The internal LDO output V_{DD} ramps up along with the input voltage. If the SIC32301 co-operates with the hot-swap controller, the V_{DD} output can be used to power up the hot-swap controller.

The power FET remains off until the ON / PD signal is pulled high. When the ON / PD signal becomes high and the 1 ms insertion delay time ends, the power FET is charged up by the internal 12 µA charge pump under the supervision of the soft-start control loop and the CLREF current limiting loop, which itself is a function of the V_{OUT}/V_{IN} voltage ratio, or alternately, the DAC output of a controller.

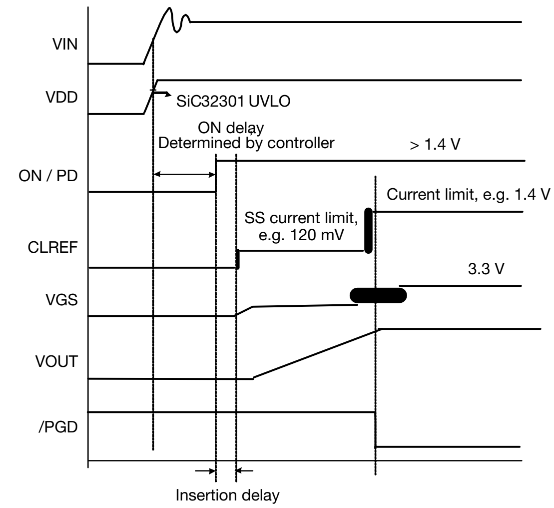


Fig. 4 - Start-Up Sequences Between SiC32301 and Front-End Control

If the SIC32301 works in stand-alone (see Fig. 5), an external capacitor (CON) can be connected from ON / PD to ground for an automatic start-up. The internal 4 µA current source charges the capacitor when V_{DD} is higher than the UVLO. Also, ON / PD can be pulled up externally to the V_{DD} voltage. A 10 µA current source of CLREF determines the current limit level through a resistor to ground.

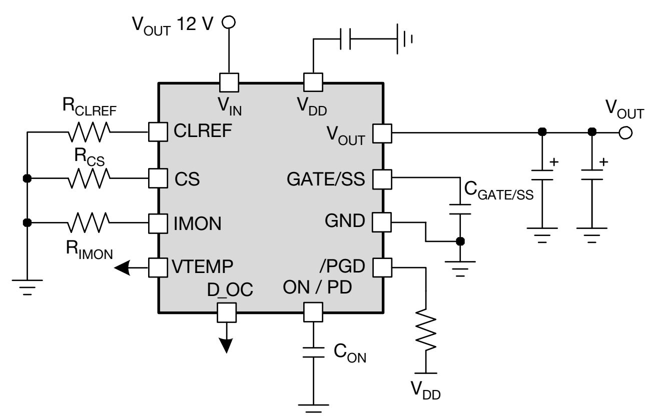


Fig. 5 - SiC32303 Schematic When Operating Standalone

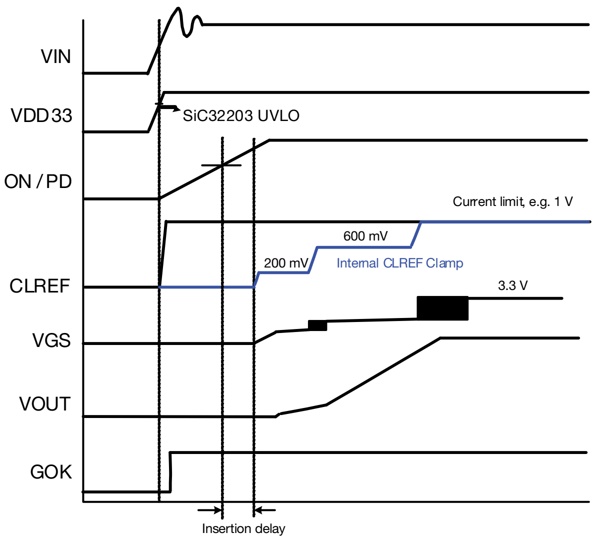


Fig. 6 - SiC32303 Schematic When Operating Standalone

Current Limit at Start-Up

The SiC32301 load current is limited by the CLREF input. The CS voltage is compared with the CLREF voltage through an OTA amplifier to regulate the power FET gate. This prevents the switch current from exceeding the CLREF defined current limit. The CLREF voltage is set and internally clamped lower during start-up to allow a controlled, gradual ramping up of V_{OUT} voltage. Once V_{OUT} is ramped **close to** $\mathbf{V_{IN}}$, the CLREF can be raised to the full current limit, the power FET gate is fully enhanced, and the system is ready to withdraw power from the input.

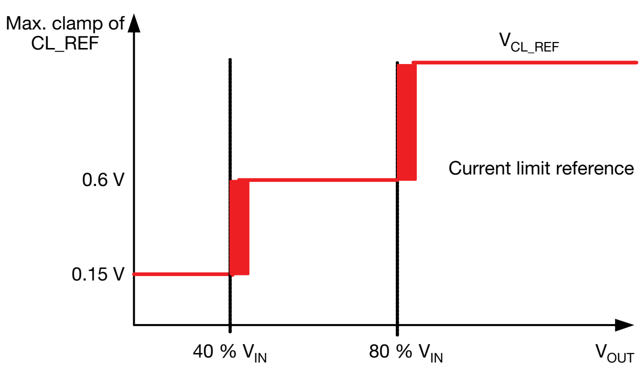


Fig. 7 - CLREF Maximum Clamp at Different V_{OUT} Levels

As shown in Fig. 7, in order to protect the device from overheating during start-up, a maximum power limit is included during start-up. The CLREF signal has an internal maximum clamp that depends on V_{IN} and V_{OUT}. When $V_{OUT} < 80\ \%\ V_{IN}$, the CLREF is clamped at 500 mV. When $V_{OUT} > 80\ \%\ V_{IN}$, the CLREF is clamped to 1.6 V. Note that the clamp is temperature compensated at -2 mV/°C if $V_{OUT} < 80\ \%\ V_{IN}$.

The desired start-up current limit is a function of the CS resistor RCS. The CLREF voltage is calculated with equation (1):

$$I_{LIMIT\_SS} = \frac{V_{CLREF\_SS}}{10\ \mu A \times R_{CS}}$$

Where V_{CLREF_SS} is the CLREF voltage at start-up. Then the V_{OUT} power-up ramp time can be approximately estimated with equation (2):

$$t_{RAMP} = \frac{V_{IN}}{10\ \mu A \times I_{LOAD}} \times C_{OUT}$$

The V_{OUT} ramp time varies with the load condition and the output capacitor (C_{OUT}) while adopting the CLREF current limit during start-up. For example, for V_{CLREF_SS} = 120 mV, RCS = 2 kΩ. The desired soft-start current limit is 6 A, that is, the maximum FET start-up current is limited to around 6 A. If C_{OUT} = 8500 µF, V_{IN} = 12 V, and the V_{OUT} ramp time is about 17 ms without an output load.

A capacitor connected to SS determines the soft-start time. When ON / PD is pulled high, a constant-current source proportional to the input voltage ramps up the voltage on SS. The output voltage rises at a similar slew rate to the SS voltage. The SS capacitor can be set larger to get a longer soft- start time. The voltage on the SS capacitor will equal 10 % of V_{OUT}. This scaling allows for an internal stabilizing feedback network between V_{OUT} and the soft-start error amplifier.

During start-up, if the CS voltage exceeds CLREF, the power FET gate voltage is regulated to hold the FET current constant. If the power FET remains on while the V_{OUT} remains lower than 90 % V_{IN} within the 200 ms maximum soft-start time, the power FET is shut down when the 200 ms time ends (see Fig. 8).

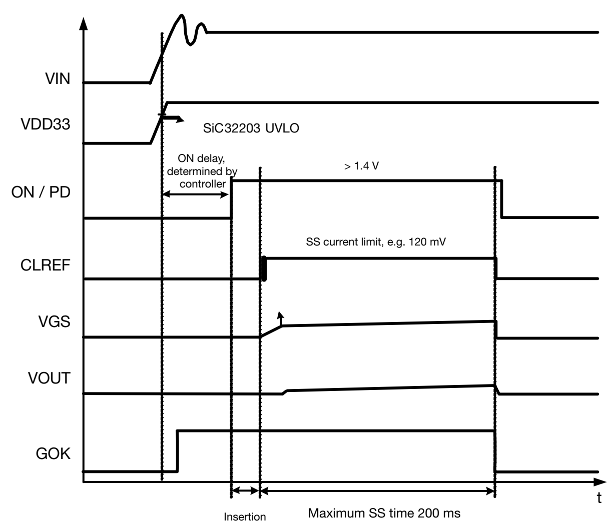


Fig. 8 - SiC32301 Start-Up at Short Circuit

Normal Operation

When the output voltage has ramped up close to V_{IN} and it remains higher than 90 % V_{IN}, the CLREF voltage will be allowed to operate at full value (not to exceed 1.6 V) and the charge pump will drive V_{GS} of the power FET to a fully enhanced condition. Fault supervision circuits will monitor the need for corrective action if needed.

Current Limit at Normal Operation

During normal operation, if the CS voltage exceeds V_{OC_TH}, which is typically 85 % of the CLREF voltage, the D_OC flag will activate (pull down current). If the CS voltage exceeds CLREF voltage for more than 250 μs, the switch will be off, and the GOK flag will latch. During this 250 μs window, the V_{GS} of the power FET remains fully enhanced unless short circuit or over-temperature fault is detected. No current limiting occurs during this 250 μs interval. If the GOK pin latches, the power supply or ON / PD will require cycling to clear the latch.

The desired current limit at normal operation is a function of the CS resistor (R_{CS}). The SIC32301 current limit value should be higher than the normal maximum load current, allowing the tolerances in the current sense value. The current limit can be set using equation (5):

$$I_{LIMIT} = \frac{V_{CLREF}}{10\ \mu A \times R_{CS}}$$

Where V_{CLREF} is the voltage of CLREF in normal operation.

For example, for V_{CLREF} = 1.2 V, R_{CS} = 2 kΩ; the desired current limit is 60 A at normal operation.

Short-Circuit Protection

Regardless of the programmed value of CLREF, if a current greater than 100 A is observed, the power FET V_{GS} is forced to 0 V rapidly (typically with 200 ns) and the GOK fault is latched. If the GOK pin latches, the power supply will require cycling to clear the latch.

ON / PD Control

ON / PD is used to control both the on/off of the internal power FET and the pull-down mode of the output voltage. When ON / PD is used for power FET on / off control, the FET is turned on if the ON / PD voltage is higher than 1.4 V. If the ON / PD voltage is lower than 1.2 V, the FET is turned off. If ON / PD is used for V_{OUT} pull- down mode, the ON / PD voltage needs to be clamped around 1.1 V for more than 80 μs. The SiC32301 recognizes 0.8 V < ON / PD < 1.2 V as a special state that requires pulling down V_{OUT}.

The ON / PD has a fixed 1 ms insertion delay after V_{DD} and V_{IN} have passed the UVLO threshold. All fault functionality is operative during the insertion delay, so that the GOK signal is pulled high if no fault is detected or remains low if a fault is detected. The ON / PD high level during this insertion delay will not turn on the switch if a fault exists. If a non-latching fault self-clears, then a 1 ms timer will begin once the ON_PD pin is above 1.4 V. Prior to V_{IN} being sufficiently high or after a latching fault event, an internal 1 MΩ resistor will attempt to discharge the ON_PD pin.

Once the ON / PD voltage is pulled higher than 1.4 V, and the insertion delay ends, the internal charge pump charges the power FET's GATE voltage allowing. Once the GATE voltage reaches its threshold (V_{GSTH}), the output voltage rises. The output voltage rises following the supervision of CLREF controlled current limit soft-start control loop (see Fig. 9) which retard the GATE voltage until V_{OUT} is sufficiently charged limited via power FET in-rush current.

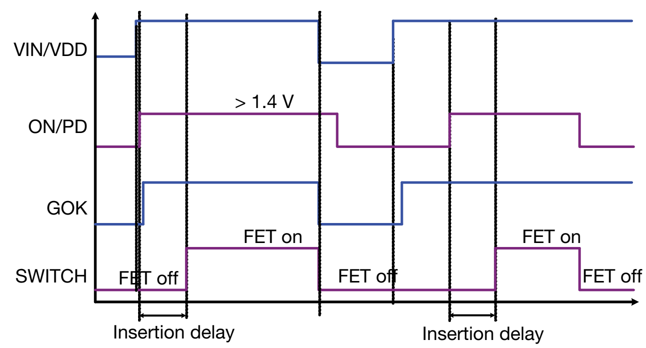


Fig. 9 - Power FET On / Off Control by ON / PD When no Fault Occurs

If the SiC32301 works in stand-alone, a capacitor on ON / PD can be used for automatic start-up by the internal 4 μA pull-up current source. Once the ON / PD voltage reaches its turn-on threshold, the power FET gate is charged by the internal 12 μA charge pump.

When the ON / PD voltage is set to around 1.1 V for more than 80 μs, the SiC32301 works in pull-down mode (see Fig. 10). In pull-down mode, when the power FET is turned off, an integrated.

500 Ω pull-down resistor attached to the output discharges the output after a fixed delay time (2.1 ms). If the ON / PD signal is pulled low directly, the pull-down mode is disabled, and the switch output voltage discharges through the external load.

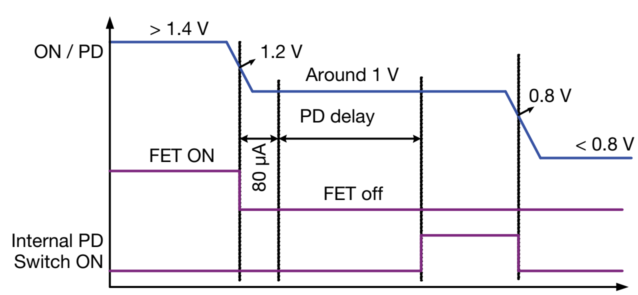


Fig. 10 - PD Mode Control by ON / PD

The connection of ON / PD is shown in Fig. 11. Pull up ON / PD to 3.3 V through a resistor divider from the controller. For example, choose R_{ON} =100 kΩ. If ON / PD is only used for the power FET on / off control, the resistor RPD in Fig. 10 can be set to 0 Ω. If a 35 kΩ R_{PD} resistor is selected, ON / PD is set to around 1 V by the external resistor divider, and the ON / PD internal 5 µA current source, which enables pull-down mode.

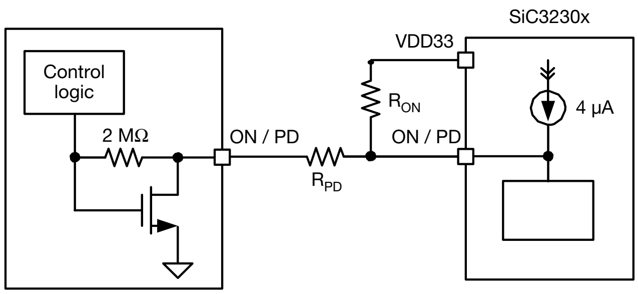


Fig. 11 - ON / PD Connection

GOK / PGD Report

GOK / PGD is an open-drain, active-low signal to report the fault of intelli-fuse. When a fault occurs, GOK is pulled low. Pull up GOK to the V_{DD} voltage through a 100 kΩ resistor. During the V_{DD} power-up, the GOK output is driven low. Before the power FET is turned on, the GOK fault condition is detected during the ON / PD 1 ms insertion delay. All fault functionality is operative during the insertion delay time, so that the GOK signal is pulled high if no fault is detected or is pulled low if a fault is detected.

GOK monitors the following fault events:

1. Over-current protection: when the CS voltage exceeds the CLREF threshold during normal operation, the GOK signal is pulled low after a 250 µs gate regulation time and latches
2. Short-circuit protection: when the load current reaches 100 A rapidly, GOK is pulled low immediately and latches
3. The integrated power FET D-S, G-D, or G-S short detection: detailed performance characteristics can be reviewed in the “Damaged Integrated Power FET Detection” section. Although these faults cause GOK / PGD to pull low immediately, the GOK / PGD pin does not latch in response to these until 200 ms has expired
4. Over-temperature protection at junction temperature TJ > 150 °C: once a fault is detected, GOK is pulled down and latches

The release of the GOK fault latch can be accomplished by re-cycling V_{IN} or by toggling ON / PD.

Fig. 12 and Fig. 13 shows the FET on / off control with the GOK timing diagram. When SiC32301 and SiC32302 are controlled by the front-end controller, the ON / PD signal will be pulled low; it is also pulled low internally by a 1 MΩ if the controller detects that GOK is latched.

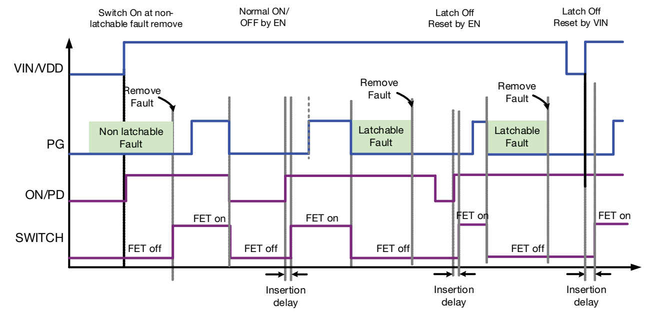


Fig. 12 - FET On / Off Control With GOK Timing Diagram

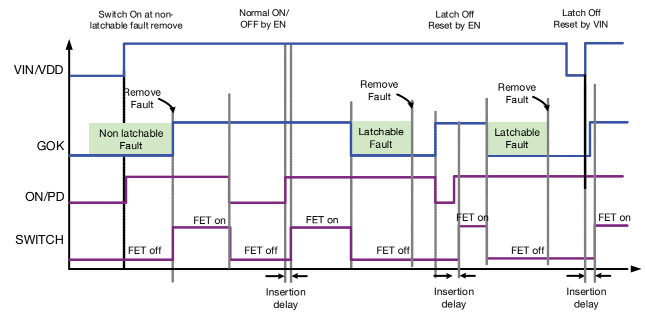


Fig. 13 - FET On / Off Control With PG Timing Diagram

Damaged Integrated Power FET Detection

The damaged integrated power FET detection includes FET drain-source short, gate-drain short, and gate-source short.

1. D-S short detection during start-up

Once the V_{DD} is higher than the UVLO rising threshold, the controller detects a shorted pass FET during power-up by treating an output voltage that exceeds 90 % x V_{IN} during power up as a short on the MOSFET. The GOK signal remains low when the controller detects V_{OUT} > 90 % x V_{IN} during start up. Once the short is removed and controller detects V_{OUT} < 70 % x V_{IN}, the GOK signal is released to high again, and the hot-swap controller prepares for normal start-up.

2. G-D short detection during start-up

During power-up, the controller detects the power FET G-D short by the condition of power FET drain-to-gate voltage (V_{GS} > 2 V). The GOK signal remains low until the short is removed, and the controller detects V_{GS} < 2 V.

3. G-S short detection during FET turn on (hot swap enable)

For G-S short detection during the FET turn-on period (if SiC32301 detects V_{OUT} is lower than 90 % x V_{IN} after the internal maximum 200 ms soft-start time), the GOK is pulled low. Remove the short and recycle V_{IN} to turn on the fuse again

4. G-S, G-D short detection during normal operation

When the part operates normally and V_{OUT} remains higher than 90 % x V_{IN}, the controller detects the power FET G-S or G-D short by the condition of V_{CP} - V_{GATE} is always lower than 2 V after 200 ms (with no other fault occurring). GOK is pulled low, where V_{CP} is the internal charge pump voltage. Remove the short and recycle V_{IN} to turn on the fuse again

The power FET short performance is listed in Table 1

TABLE 1 - THE POWER FET SHORT PERFORMANCE

FET FAULT PERFORMANCE		DETECTION CONDITION	GOK FLAG
Start-up FET short	D - S	V_{OUT} > 90 % x V_{IN}	Keep low until V_{OUT} < 70 % x V_{IN}
	G - D	V_{GS} > 2 V	Keep low until V_{GS} < 2 V
	G - S	V_{OUT} > 90 % x V_{IN} after 200 ms	Pull low
Normal operation FET short	G - D / G - S	(V_{CP} - V_{GATE}) < 2 V after 200 ms	Pull low

D_OC Report

D_OC is an open-drain, active-low output to report the over-current fault. When the voltage on CS is higher than V_{OC_TH}, typically 85 % of CLREF, the D_OC is driven low. Pull up D_OC to the VDD voltage through a 100 k? resistor.

Input and Output Transient Protection

The hot-swap system experiences positive transients on the input during a hot plug or rapid turn off with high current due to parasitic inductance in the input circuit.

For input transient protection, a TVS diode (transient voltage suppressor, a type of Zener diode) may be required on the input to limit transient voltages below the absolute maximum ratings.

The output may experience negative transients during rapid turn off with high current due to inductance in the output circuit. The lowest voltage allowed on the device pins is a -0.3 V_{DC} rating and a -1 V for 100 ns AC rating. If a transient makes OUT more negative, the internal ESD Zener diode attached to the pin will become forward biased, and the current will be conducted across the substrate to the ground. The internal ESD diode may not be strong enough to sustain a large current, and the current may disrupt normal operation or, if large enough, damage the part.

An output voltage clamp diode may be required on the output to limit negative transients. Select a Schottky diode with a low forward voltage at the anticipated current during an output short. By doing this, the negative voltage spike at the output terminal can be clamped at less than -0.7 V, thus the IC is protected during a short output.

Current Sense (CS Output)

CS provides a current proportional to the output current (the current through the power device). The gain of the current sense is 10 µA/A.

There is a resistor (R_{CS}) connected from CS to form an external voltage. Use equation (6) and equation (7) to determine a proper reference voltage:

$I_{CS} = I_{OUT} \times 10\ \mu A/A$ (6)

$V_{CS} = I_{CS} \times R_{CS}$ (7)

Once the CS voltage reaches the CLREF current limit threshold, the internal circuit regulates the gate voltage to hold the current in the power FET constant.

Current Monitor (I_{MON} Output)

The gain of the current monitor is 10 µA/A. There is a resistor (R_{IMON}), connected from I_{MON} to ground. The I_{MON} voltage range of 0 V to 1.6 V is required to keep I_{MON}'s output current linearly proportional to the output current use equation (8) and equation (9) to determine a proper reference voltage:

$I_{MON} = I_{OUT} \times 10\ \mu A/A$ (8)

$V_{IMON} = I_{MON} \times R_{IMON}$ (9)

The current monitor output can be used by the controller to monitor accurately the output current. Place a 100 nF capacitor from I_{MON} to GND to smooth the indicator voltage.

Generally, connect a 2 kΩ resistor (R_{IMON}) to ground to set the gain of the output, which is about 20 mV per ampere. For best accuracy, use resistors within 1 percent.

Temperature Sense Output, V_{TEMP}

V_{TEMP} reports the junction temperature. It is a voltage output proportional to the junction temperature. The V_{TEMP} output voltage is 10 mV/°C with a 200 mV offset. See equation (10):

$V_{TEMP} = T_{JUNCTION} \times 10\ mV + 200\ mV$ (10)

For example, if the junction temperature is 100 °C, the V_{TEMP} voltage is 1.2 V. If V_{TEMP} = 0 V, the junction temperature is about -20 °C. The total temperature sense range is -20 °C to +140 °C. When the junction temperature is below -20 °C, V_{TEMP} remains at 0 V.

In multi-fuse operation, V_{TEMP} pins of every paralleled fuse can be connected to the temperature monitor pin of the controller (see Fig. 14).

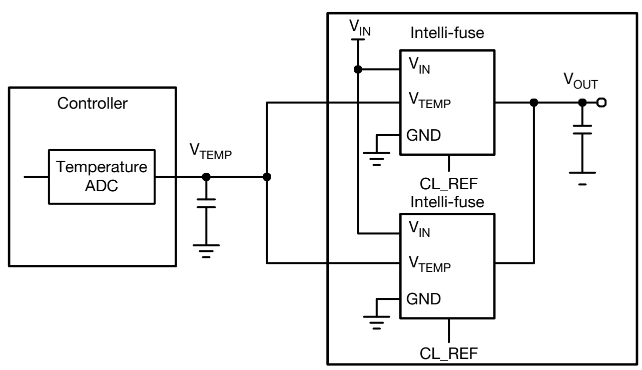


Fig. 14 - Multi-Fuse Temperature Sense Utilization

Thermal Protection

The device temperature is sensed by monitoring internally the junction temperature of the IC. The temperature information can be read from V_{TEMP}.

The device itself has thermal protection. When the junction temperature exceeds the threshold (150 °C), the power FET is turned off, and GOK is pulled low.

UVLO Protection

The SiC32301 has two under-voltage lockout protections: a V_{DD} UVLO and a V_{IN} UVLO. The part can start up only when both the V_{DD} and V_{IN} exceed their own UVLO. The part shuts down when either the V_{DD} voltage is lower than the UVLO falling threshold voltage (typically), or the V_{IN} is lower than the V_{IN} falling threshold. Both UVLO protections are non-latching off.

APPLICATION SCHEMATICS

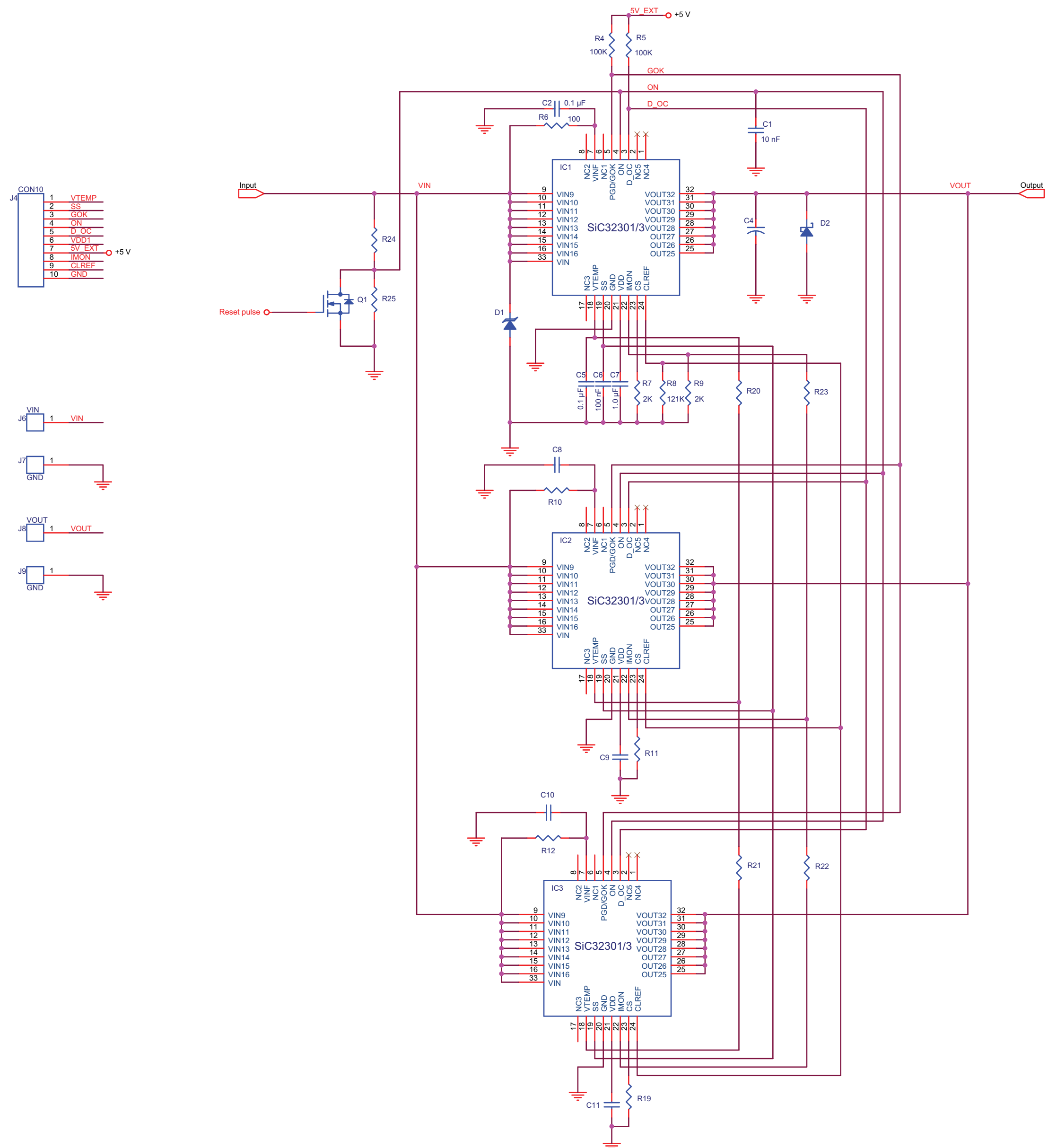


Fig. 15 - SiC32301, 32303 (Latch Logic), Parallel Fuse Operation With Controller

The ON pin can interface with micro-processor for on / off and discharge control. Toggle the ON pin will reset the fuse from latch logic status.

In case the on is connected to a V_{IN} voltage divider formed by R_{24} and R_{25}, applying a pulse at Q1 will reset the fuse.

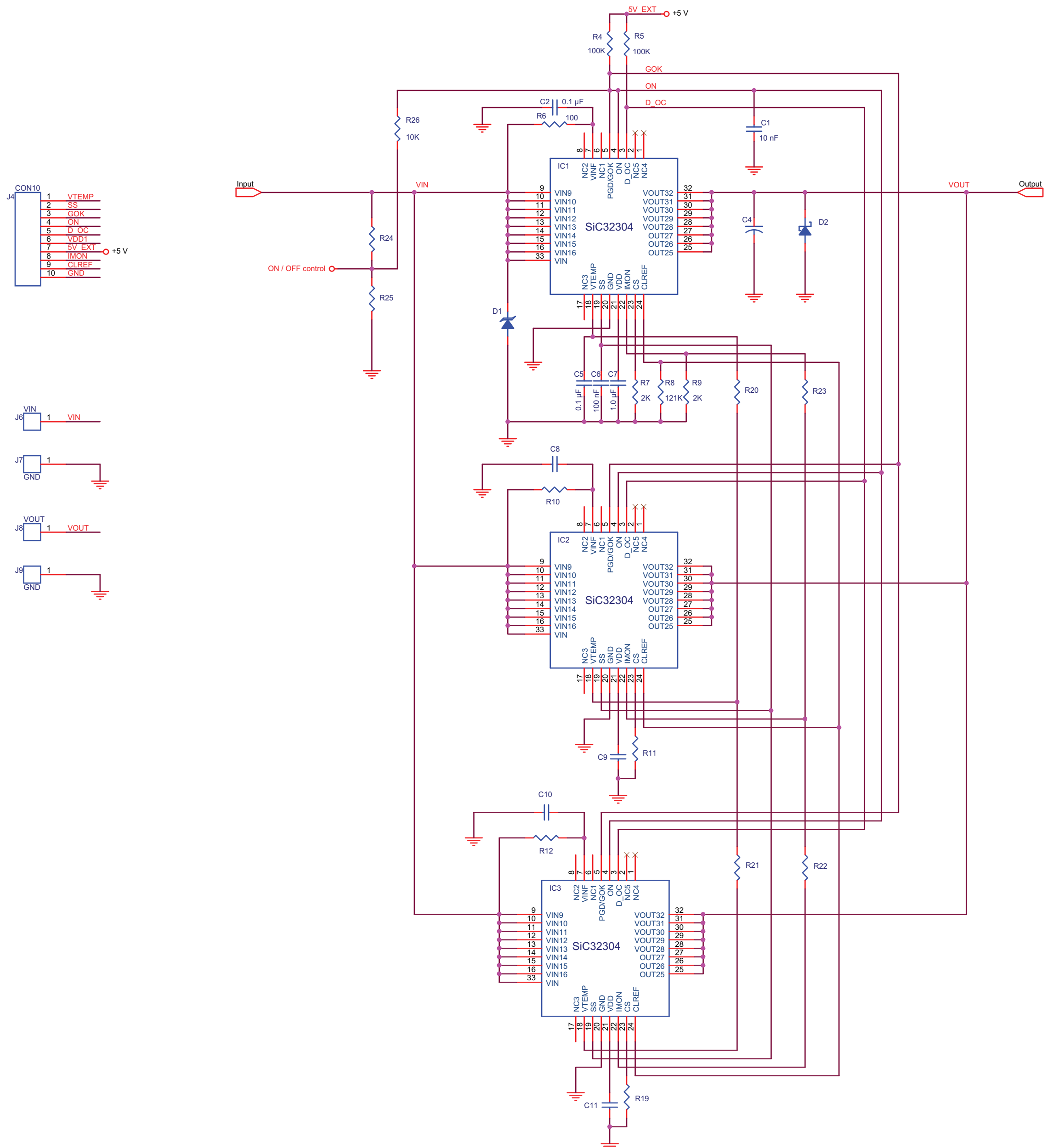


Fig. 16 - SiC32304 (Auto-Retry Logic), Parallel Fuse Operation With Controller

The ON pin can interface with micro-processor for on / off and discharge control.

The parallel fuse on can be controlled with the V_{IN} voltage divider.

Connect GOK to ON with those parallel fuse of auto-retry logic.

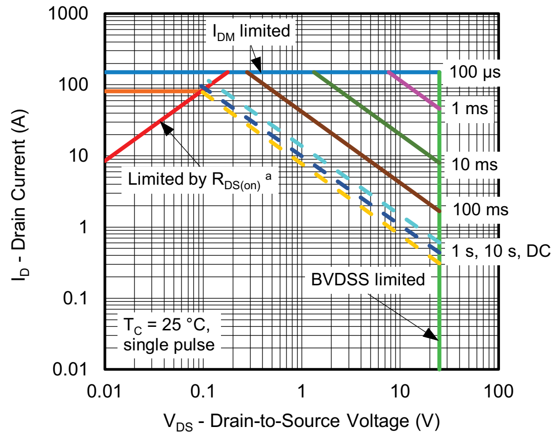


Fig. 17 - Safe Operating Area Curve

PRODUCT SUMMARY				
Part number	SiC32301	SiC32302	SiC32303	SiC32304
Description	0.6 mΩ, hot-swap eFuse, I_{MON}, PGD, D_OC report latch on fault	0.6 mΩ, hot-swap eFuse, I_{MON}, PGD, D_OC report latch on fault	0.6 mΩ, hot-swap eFuse, I_{MON}, PGD, D_OC report latch on fault	0.6 mΩ, hot-swap eFuse, I_{MON}, PGD, D_OC report latch on fault
Configuration	Parallable	Parallable	Parallable	Parallable
Slew rate time (µs)	Adjustable	Adjustable	Adjustable	Adjustable
On delay time (µs)	1000	1000	1000	1000
Input voltage min. (V)	4.5	4.5	4.5	4.5
Input voltage max. (V)	25	25	25	25
On-resistance at input voltage min. (mΩ)	0.6	0.6	0.6	0.6
On-resistance at input voltage max. (mΩ)	0.6	0.6	0.6	0.6
Quiescent current at input voltage min. (µA)	2100	2100	2100	2100
Quiescent current at input voltage max. (µA)	2800	2800	2800	2800
Output discharge (yes / no)	Yes	Yes	Yes	Yes
Reverse blocking (yes / no)	No	No	No	No
Continuous current (A)	60	50	60	50
Package type	MLP55-32	MLP55-32	MLP55-32	MLP55-32
Package size (W, L, H) (mm)	5 x 5 x 0.8	5 x 5 x 0.8	5 x 5 x 0.8	5 x 5 x 0.8
Status code	-	-	-	-
Product type	Hot swap, eFuse, slew rate, current report	Hot swap, eFuse, slew rate, current report	Hot swap, eFuse, slew rate, current report	Hot swap, eFuse, slew rate, current report
Applications	Computers, telecom, industrial	Computers, telecom, industrial	Computers, telecom, industrial	Computers, telecom, industrial

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