# Si4178DY

RoHS

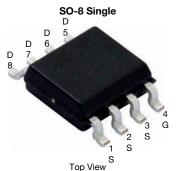
COMPLIANT

HALOGEN

FREE

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Vishay Siliconix



2 S 1 S Top View					
PRODUCT SUMMARY					
V <sub>DS</sub> (V)	30				
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS}$ = 10 V	0.021				
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS}$ = 4.5 V	0.033				
Q <sub>g</sub> typ. (nC)	3.7				
I <sub>D</sub> (A) <sup>a</sup>	12				
Configuration	Single				

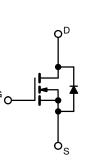
#### **FEATURES**

N-Channel 30 V (D-S) MOSFET

- TrenchFET® power MOSFET
- 100% R<sub>g</sub> and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

#### **APPLICATIONS**

- Notebook system power
- Low current DC/DC



N-Channel MOSFET

#### **ORDERING INFORMATION**

Package	SO-8
Lead (Pb)-free and halogen-free	Si4178DY-T1-GE3

ABSOLUTE MAXIMUM RATING	(·A, -	1		LINUT	
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V <sub>DS</sub>	30	V	
Gate-source voltage		V <sub>GS</sub>	± 25	V	
	T <sub>C</sub> = 25 °C		12 <sup>a</sup>		
Continuous drain current ( $T_J = 150 \ ^\circ C$ )	T <sub>C</sub> = 70 °C		9.7 <sup>a</sup>		
	T <sub>A</sub> = 25 °C	I <sub>D</sub>	8.3 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C		6.7 <sup>b, c</sup>		
Pulsed drain current		I <sub>DM</sub>	40	A	
Continuous source-drain diode current	T <sub>C</sub> = 25 °C		4.2		
	T <sub>A</sub> = 25 °C	I <sub>S</sub>	2 <sup>b, c</sup>		
Single pulse avalanche current		I <sub>AS</sub>	10		
Single pulse avalanche energy	L = 0.1 mH	E <sub>AS</sub>	5	mJ	
Maximum power dissipation	T <sub>C</sub> = 25 °C		5		
	T <sub>C</sub> = 70 °C		3.2	w	
	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2.4 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C	1	1.5 <sup>b, c</sup>		
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C	

#### THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT	
PARAMETER		STINDUL	TTPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient b, d	$t \le 10 s$	R <sub>thJA</sub>	42	53	°C AM	
Maximum junction-to-foot (drain)	Steady state	R <sub>thJF</sub>	19	25	°C/W	

#### Notes

a. Package limited

b. Surface mounted on 1" x 1" FR4 board

c. t = 10 s

d. Maximum under steady state conditions is 85 °C/W

S10-0212-Rev. A, 25-Jan-10

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## Si4178DY

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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static			•		•		
Drain-source breakdown voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$	30	-	-	V	
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	L 050 A	-	25	-		
V <sub>GS(th)</sub> temperature coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA	-	-6	-	mV/°C	
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \ \mu A$	1.4	-	2.8	V	
Gate-source leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 25 V$	-	-	± 100	nA	
Zaus ante colta de sin sumont		$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	-	1	uA uA	
Zero gate voltage drain current	I <sub>DSS</sub>	$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 55 ^{\circ}\text{C}$	-	-	10		
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, \text{ V}_{GS} = 10 \text{ V}$	20	-	-	А	
	_	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 8.4 \text{ A}$	-	0.017	0.021		
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 2 \text{ A}$	-	0.027	0.033	Ω	
Forward transconductance a	9 <sub>fs</sub>	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 8.4 \text{ A}$	-	22	-	S	
Dynamic <sup>b</sup>			•		•		
Input capacitance	C <sub>iss</sub>		-	405	-	pF	
Output capacitance	C <sub>oss</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	110	-		
Reverse transfer capacitance	C <sub>rss</sub>		-	56	-		
Total gate charge	Qg	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 8.4 \text{ A}$	-	7.5	12		
			-	3.7	5.6		
Gate-source charge	Q <sub>qs</sub>	$V_{DS}$ = 15 V, $V_{GS}$ = 4.5 V, $I_{D}$ = 8.4 A	-	1.6	-	- nC	
Gate-drain charge	Q <sub>gd</sub>		-	1.3	-		
Gate resistance	R <sub>g</sub>	f = 1 MHz	0.5	2.6	5.2	Ω	
Turn-on delay time	t <sub>d(on)</sub>		-	20	30	-	
Rise time	t <sub>r</sub>	$V_{DD} = 15 \text{ V}, \text{ R}_{L} = 2.2 \Omega$	-	15	25		
Turn-off delay time	t <sub>d(off)</sub>	$I_D \cong 6.7$ Å, $V_{GEN} = 4.5$ V, $R_g = 1 \ \Omega$	-	11	20		
Fall time	t <sub>f</sub>		-	10	15		
Turn-on delay time	t <sub>d(on)</sub>		-	7	15	ns	
Rise time	t <sub>r</sub>	$V_{DD}$ = 15 V, RL = 2.2 $\Omega$	-	10	15		
Turn-off delay time	t <sub>d(off)</sub>	$I_D \cong 6.7$ Å, $V_{GEN} = 10$ V, $R_g = 1$ $\Omega$	-	12	20		
Fall time	t <sub>f</sub>		-	10	15		
Drain-Source Body Diode Characteristic	cs		•		•		
Continuous source-drain diode current	IS	T <sub>C</sub> = 25 °C	-	-	4.2		
Pulse diode forward current	I <sub>SM</sub>		-	-	40	A	
Body diode voltage	V <sub>SD</sub>	$I_{\rm S} = 6.7$ A, $V_{\rm GS} = 0$ V	-	0.85	1.2	V	
Body diode reverse recovery time	t <sub>rr</sub>		-	15	30	ns	
Body diode reverse recovery charge	Q <sub>rr</sub>	I <sub>F</sub> = 6.7 A, di/dt = 100 A/μs,	-	8	16	nC	
Reverse recovery fall time	ta	$T_{\rm J} = 25 \ ^{\circ}{\rm C}$	-	8.5	-		
Reverse recovery rise time	t <sub>b</sub>		-	6.5	-	ns	

Notes

a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2%

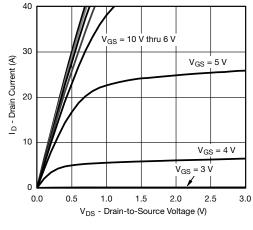
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

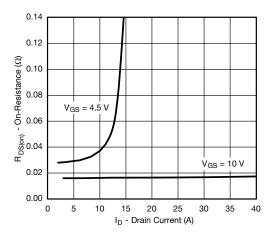
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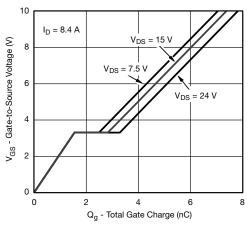
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



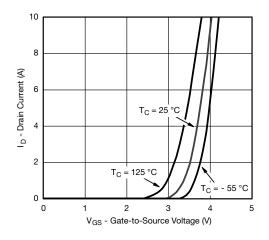
**Output Characteristics** 



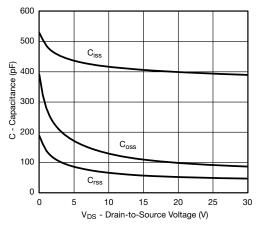
**On-Resistance vs. Drain Current** 



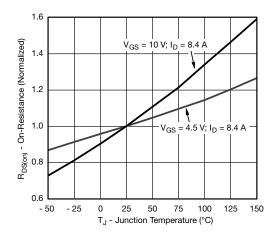
**Gate Charge** 



**Transfer Characteristics** 



Capacitance

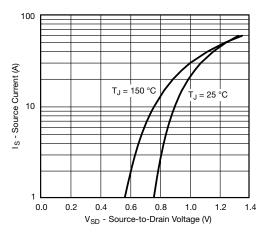


**On-Resistance vs. Junction Temperature** 

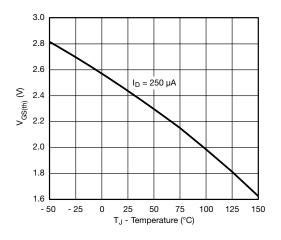
3



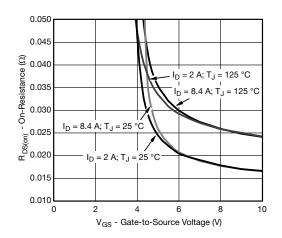
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



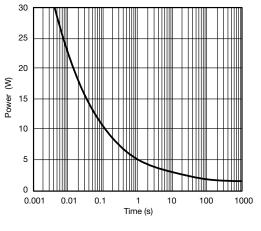
Source-Drain Diode Forward Voltage



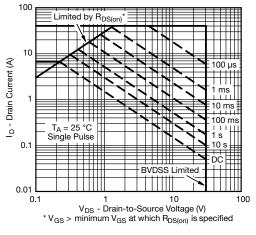
**Threshold Voltage** 



**On-Resistance vs. Gate-to-Source Voltage** 





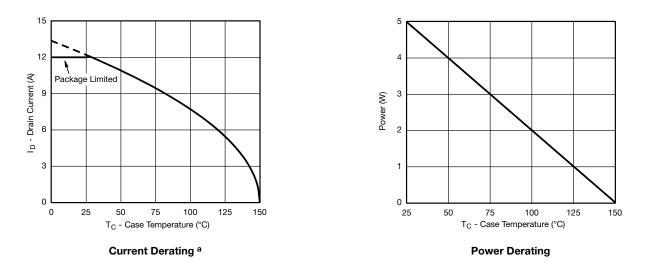


Safe Operating Area, Junction-to-Ambient

4



### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

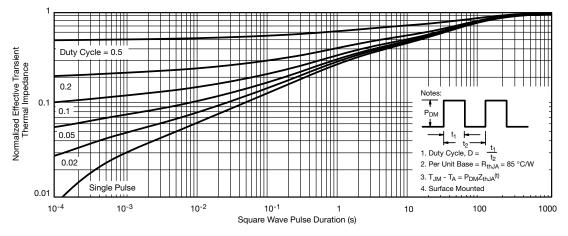


#### Note

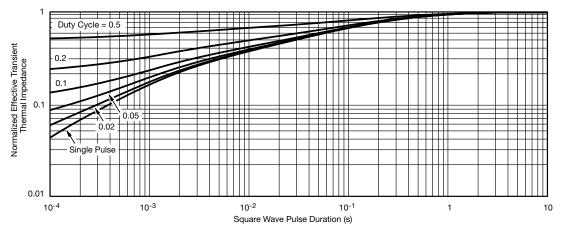
a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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# Package Information

Vishay Siliconix

# SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012





	MILLIM	IETERS	INC	HES	
DIM	Min	Мах	Min	Max	
A	1.35	1.75	0.053	0.069	
A <sub>1</sub>	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27	BSC	0.050 BSC		
н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498					

## **Application Note 826**

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**RECOMMENDED MINIMUM PADS FOR SO-8** 



Recommended Minimum Pads Dimensions in Inches/(mm)

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