SPICE Device Model SQ1470AEH



Vishay Siliconix

N-Channel 30 V (D-S) 175 °C MOSFET

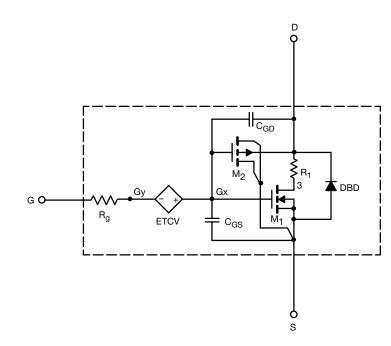
DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Sub-circuit Model)
- Level 3 MOS
- · Apply for both Linear and Switching Application
- Accurate over the -55 °C to +125 °C Temperature Range
- Model the Gate Charge



SUBCIRCUIT MODEL SCHEMATIC

Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	V _{GS(th)}	$V_{DS}=V_{GS},\ I_{D}=250\ \mu A$	0.9	1	V
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS}=4.5 \text{ V}, \text{ I}_{D}=4.2 \text{ A}$	0.045	0.045	Ω
		$V_{GS} = 2.5 \text{ V}, \text{ I}_{D} = 4.2 \text{ A}$	0.060	0.060	
Forward Transconductance ^a	g _{fs}	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 1.7 \text{ A}$	11	14	S
Diode Forward Voltage	V _{SD}	I _S = 1.7 A	0.73	0.70	V
Dynamic ^b					
Input Capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	326	350	pF
Output Capacitance	C _{oss}		68	65	
Reverse Transfer Capacitance	C _{rss}		33	30	
Total Gate Charge	Qg	V_{DS} = 15 V, V_{GS} = 4.5 V, I_{D} = 4.2 A	3.2	4.2	nC
Gate-Source Charge	Q _{gs}		1.1	1.1	
Gate-Drain Charge	Q _{gd}		0.7	0.7	

Notes

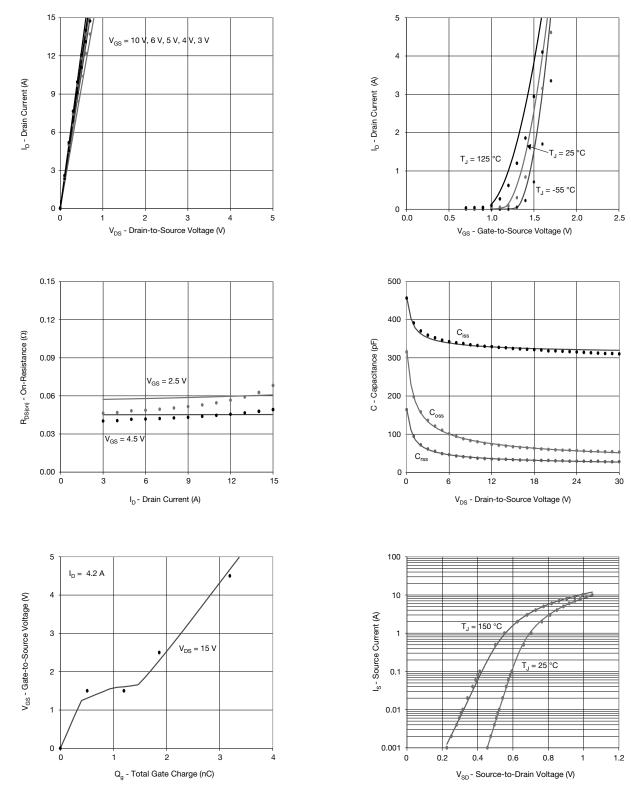
a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.



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COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)



Note

• Dots and squares represent measured data. Copyright: Vishay Intertechnology, Inc.

S15-0952-Rev. A, 27-Apr-15

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Document Number: 65772

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