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Vishay Siliconix

# Automotive P-Channel 30 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	-30			
$R_{DS(on)}(\Omega)$ at $V_{GS} = -10 \text{ V}$	0.175			
$R_{DS(on)}(\Omega)$ at $V_{GS} = -4.5 \text{ V}$	0.300			
I <sub>D</sub> (A)	-3			
Configuration	Single			
Package	SC-70			

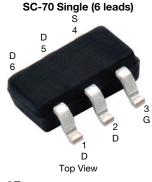
#### **FEATURES**

- TrenchFET® power MOSFET
- AEC-Q101 qualified c
- 100 % R<sub>q</sub> and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912









Marking Code: 9E

G <b>o</b>	S S
P-Channel MOSFET	D

ABSOLUTE MAXIMUM RATINGS	$(T_C = 25  ^{\circ}C, \text{ unles})$	s otherwise noted	d)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		$V_{DS}$	-30	V	
Gate-Source Voltage		$V_{GS}$	± 20	V	
Continuous Drain Current	T <sub>C</sub> = 25 °C	L	-3		
Continuous Diain Current	T <sub>C</sub> = 125 °C	I <sub>D</sub>	-1.8		
Continuous Source Current (Diode Conduction)		I <sub>S</sub>	-3.7	Α	
Pulsed Drain Current <sup>a</sup>		$I_{DM}$	-12		
Single Pulse Avalanche Current  L = 0.1 mH		I <sub>AS</sub>	-6		
Single Pulse Avalanche Energy	L = 0.1 IIIH	E <sub>AS</sub>	1.8	mJ	
Maximum Power Dissipation <sup>a</sup>	$T_C = 25 ^{\circ}C$ $P_D$ $W$		۱۸/		
maximum r ower bissipation -	T <sub>C</sub> = 125 °C	ı-D	1	V V	
Operating Junction and Storage Temperature	Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 175	°C	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount <sup>b</sup>	$R_{thJA}$	130	°C/W
Junction-to-Foot (Drain)		$R_{thJF}$	50	G/VV

### **Notes**

- a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.
- b. When mounted on 1" square PCB (FR4 material).
- c. Parametric verification ongoing.



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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static	1 2 2 2	1					
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> =	: 0 V, I <sub>D</sub> = -250 μA	-30	-	-	.,
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-1	-1.5	-2	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	$0 \text{ V}, \text{V}_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA
		$V_{GS} = 0 V$	V <sub>DS</sub> = -30 V	-	-	-1	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -30 V, T <sub>J</sub> = 125 °C	-	-	-50	μΑ
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -30 V, T <sub>J</sub> = 175 °C	-	-	-150	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = -10 V	$V_{DS} \le -5 \text{ V}$	-5	-	-	Α
		V <sub>GS</sub> = -10 V	I <sub>D</sub> = -2 A	1	0.125	0.175	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V	I <sub>D</sub> = -2 A, T <sub>J</sub> = 125 °C	1	-	0.252	
		V <sub>GS</sub> = -10 V	I <sub>D</sub> = -2 A, T <sub>J</sub> = 175 °C	-	-	0.294	Ω
		V <sub>GS</sub> = -4.5 V	I <sub>D</sub> = -1.6 A	-	0.230	0.300	
Forward Transconductance b	g <sub>fs</sub>	V <sub>DS</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -2 A		3	-	S
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>			-	164	205	
Output Capacitance	Coss	$V_{GS} = 0 V$	$V_{DS} = -25 \text{ V}, f = 1 \text{ MHz}$	-	44	55	pF
Reverse Transfer Capacitance	C <sub>rss</sub>			1	28	35	
Total Gate Charge c	Qg			1	4.2	6.5	
Gate-Source Charge <sup>c</sup>	$Q_{gs}$	$V_{GS} = -4.5 \text{ V}$	$V_{DS} = -15 \text{ V}, I_D = -2.2 \text{ A}$	1	0.7	-	nC
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			1	1	-	]
Gate Resistance	$R_{g}$	f = 1 MHz		4.5	12.5	18.5	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			1	5	8	
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD}$ = -15 V, $R_L$ = 15 $\Omega$ $I_D \cong$ -1 A, $V_{GEN}$ = -10 V, $R_g$ = 1 $\Omega$		1	8	12	- ns
Turn-Off Delay Time c	t <sub>d(off)</sub>			1	11	17	
Fall Time <sup>c</sup>	t <sub>f</sub>			1	8	12	
Source-Drain Diode Ratings and Chara	acteristics <sup>b</sup>						
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			ı	-	-12	Α
Forward Voltage	$V_{SD}$	I <sub>F</sub> =	-1.2 A, V <sub>GS</sub> = 0 V	-	-0.85	-1.2	V

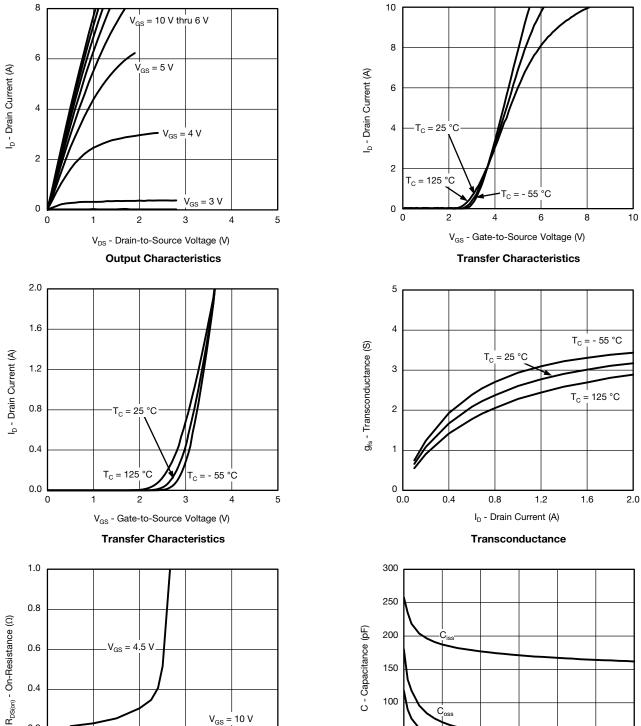
#### Notes

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



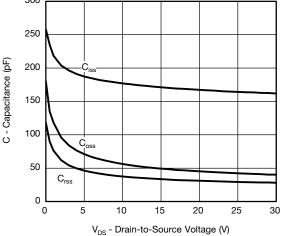
## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



 $V_{GS} = 10 \text{ V}$ 2

 $V_{GS} = 4.5 \text{ V}$ 

I<sub>D</sub> - Drain Current (A) On-Resistance vs. Drain Current



Capacitance

0.6

0.4

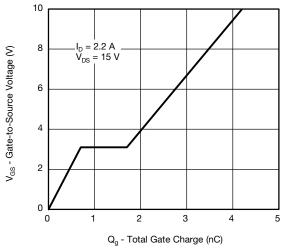
0.2

0

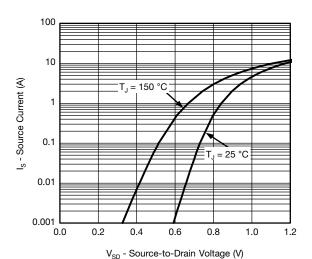
For technical questions, contact: automostechsu



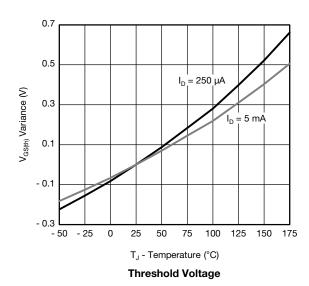
## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

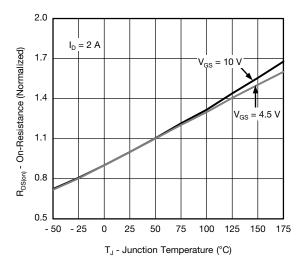


### Gate Charge

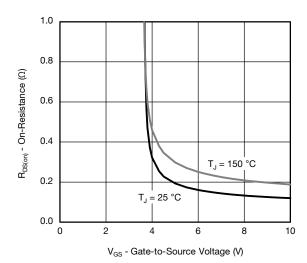


**Source Drain Diode Forward Voltage** 

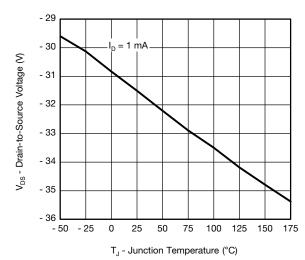




On-Resistance vs. Junction Temperature



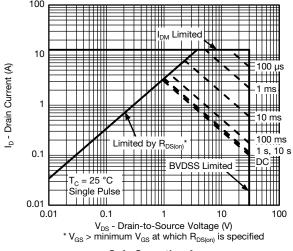
On-Resistance vs. Gate-to-Source Voltage



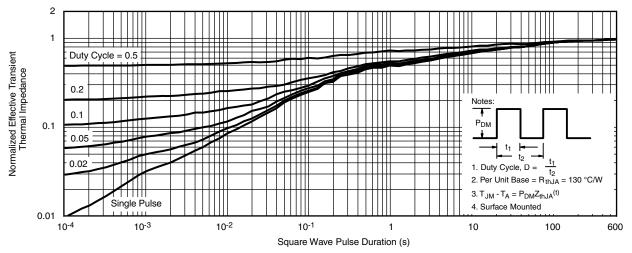
Drain Source Breakdown vs. Junction Temperature



# THERMAL RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)



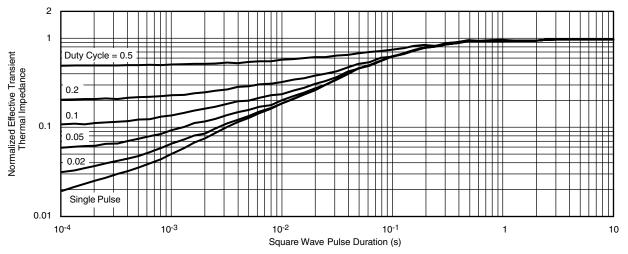
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

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### THERMAL RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Foot

#### Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Foot (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg267048">www.vishay.com/ppg267048</a>.





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REVISION HISTORY <sup>a</sup>				
REVISION	DATE	DESCRIPTION OF CHANGE		
С	03-Dec-15	Changed R <sub>g</sub> minimum		

#### Note

a. As of April 2014





### SC-70: 6-LEADS





Dim	MIL	LIMET	ERS	INCHES		
	Min	Nom	Max	Min	Nom	Max
Α	0.90	-	1.10	0.035	_	0.043
A <sub>1</sub>	-	-	0.10	-	-	0.004
$A_2$	0.80	-	1.00	0.031	-	0.039
b	0.15	-	0.30	0.006	_	0.012
С	0.10	-	0.25	0.004	_	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
Ε	1.80	2.10	2.40	0.071	0.083	0.094
E <sub>1</sub>	1.15	1.25	1.35	0.045	0.049	0.053
е		0.65BSC			0.026BSC	;
e <sub>1</sub>	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
9	7°Nom				7°Nom	



### **RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead**



Recommended Minimum Pads Dimensions in Inches/(mm)

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