

Automotive Dual N-Channel 20 V (D-S) 175 °C MOSFETs

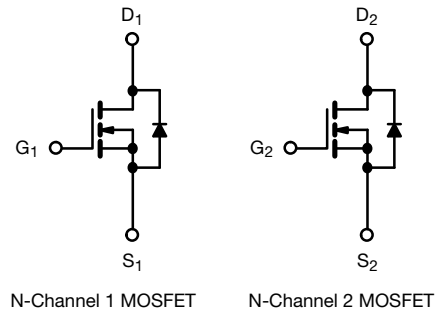
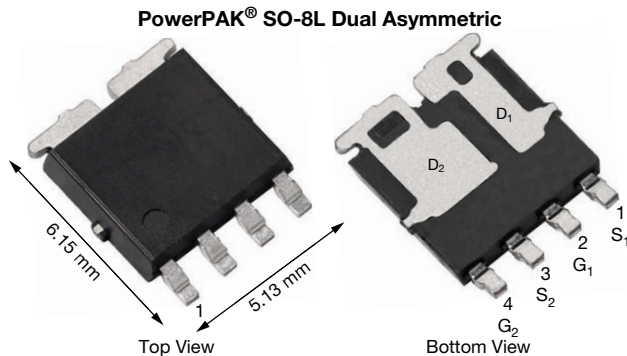
 AUTOMOTIVE
GRADE

RoHS
COMPLIANT
HALOGEN
FREE

PRODUCT SUMMARY		
	N-CHANNEL 1	N-CHANNEL 2
V_{DS} (V)	20	20
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.0088	0.0037
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5$ V	0.0124	0.0050
I_D (A)	20	60
Configuration	Dual N	
Package	PowerPAK SO-8L Dual Asymmetric	

FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified ^d
- 100 % R_g and UIS tested
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)					
PARAMETER	SYMBOL	N-CHANNEL 1	N-CHANNEL 2	UNIT	
Drain-Source Voltage	V_{DS}	20	20	V	
Gate-Source Voltage	V_{GS}	± 20			
Continuous Drain Current ^a	I_D	$T_C = 25$ °C	20	60	A
		$T_C = 125$ °C	20	50	
Continuous Source Current (Diode Conduction)	I_S	20 ^a	44		
Pulsed Drain Current ^b	I_{DM}	80	180		
Single Pulse Avalanche Current	I_{AS}	L = 0.1 mH	22	40	mJ
Single Pulse Avalanche Energy			E_{AS}	24.2	
Maximum Power Dissipation ^b	P_D	$T_C = 25$ °C	27	48	W
		$T_C = 125$ °C	9	16	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175			°C
Soldering Recommendations (Peak Temperature) ^{e, f}		260			

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	N-CHANNEL 1	N-CHANNEL 2	UNIT	
Junction-to-Ambient	R_{thJA}	85	85	°C/W	
Junction-to-Case (Drain)					

Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR4 material).
- Parametric verification ongoing.
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)								
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		N-Ch 1	20	-	-	V
		$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		N-Ch 2	20	-	-	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		N-Ch 1	1	1.5	2	
		$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		N-Ch 2	1	1.5	2	
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$		N-Ch 1	-	-	± 100	nA
				N-Ch 2	-	-	± 100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 20\text{ V}$	N-Ch 1	-	-	1	μA
		$V_{GS} = 0\text{ V}$	$V_{DS} = 20\text{ V}$	N-Ch 2	-	-	1	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 20\text{ V}, T_J = 125\text{ }^\circ\text{C}$	N-Ch 1	-	-	50	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 20\text{ V}, T_J = 125\text{ }^\circ\text{C}$	N-Ch 2	-	-	50	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 20\text{ V}, T_J = 175\text{ }^\circ\text{C}$	N-Ch 1	-	-	150	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 20\text{ V}, T_J = 175\text{ }^\circ\text{C}$	N-Ch 2	-	-	150	
On-State Drain Current ^a	$I_{D(on)}$	$V_{GS} = 10\text{ V}$	$V_{DS} \geq 5\text{ V}$	N-Ch 1	20	-	-	A
		$V_{GS} = 10\text{ V}$	$V_{DS} \geq 5\text{ V}$	N-Ch 2	30	-	-	
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 16\text{ A}$	N-Ch 1	-	0.0074	0.0088	Ω
		$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}$	N-Ch 2	-	0.0031	0.0037	
		$V_{GS} = 10\text{ V}$	$I_D = 16\text{ A}, T_J = 125\text{ }^\circ\text{C}$	N-Ch 1	-	0.0110	-	
		$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}, T_J = 125\text{ }^\circ\text{C}$	N-Ch 2	-	0.0036	-	
		$V_{GS} = 10\text{ V}$	$I_D = 16\text{ A}, T_J = 175\text{ }^\circ\text{C}$	N-Ch 1	-	0.0124	-	
		$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}, T_J = 175\text{ }^\circ\text{C}$	N-Ch 2	-	0.0063	-	
		$V_{GS} = 4.5\text{ V}$	$I_D = 14\text{ A}$	N-Ch 1	-	0.0095	0.0124	
		$V_{GS} = 4.5\text{ V}$	$I_D = 19\text{ A}$	N-Ch 2	-	0.0039	0.0050	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 10\text{ A}$		N-Ch 1	-	55	-	S
		$V_{DS} = 10\text{ V}, I_D = 10\text{ A}$		N-Ch 2	-	60	-	
Dynamic ^b								
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 10\text{ V}, f = 1\text{ MHz}$	N-Ch 1	-	723	975	pF
		$V_{GS} = 0\text{ V}$	$V_{DS} = 10\text{ V}, f = 1\text{ MHz}$	N-Ch 2	-	1937	2525	
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 10\text{ V}, f = 1\text{ MHz}$	N-Ch 1	-	269	675	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 10\text{ V}, f = 1\text{ MHz}$	N-Ch 2	-	655	870	
Reverse Transfer Capacitance	C_{rss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 10\text{ V}, f = 1\text{ MHz}$	N-Ch 1	-	112	340	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 10\text{ V}, f = 1\text{ MHz}$	N-Ch 2	-	264	350	
Total Gate Charge ^c	Q_g	$V_{GS} = 10\text{ V}$	$V_{DS} = 10\text{ V}, I_D = 20\text{ A}$	N-Ch 1	-	12	18	nC
		$V_{GS} = 10\text{ V}$	$V_{DS} = 10\text{ V}, I_D = 60\text{ A}$	N-Ch 2	-	29	43	
Gate-Source Charge ^c	Q_{gs}	$V_{GS} = 10\text{ V}$	$V_{DS} = 10\text{ V}, I_D = 20\text{ A}$	N-Ch 1	-	1.6	-	
		$V_{GS} = 10\text{ V}$	$V_{DS} = 10\text{ V}, I_D = 60\text{ A}$	N-Ch 2	-	4.1	-	
Gate-Drain Charge ^c	Q_{gd}	$V_{GS} = 10\text{ V}$	$V_{DS} = 10\text{ V}, I_D = 20\text{ A}$	N-Ch 1	-	2.5	-	
		$V_{GS} = 10\text{ V}$	$V_{DS} = 10\text{ V}, I_D = 60\text{ A}$	N-Ch 2	-	6	-	
Gate Resistance	R_g	$f = 1\text{ MHz}$		N-Ch 1	1.1	2.3	3.5	Ω
				N-Ch 2	0.4	1	1.4	



SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 6\text{ V}, R_L = 0.3\ \Omega$ $I_D \cong 20\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$	N-Ch 1	-	4	6	ns
		$V_{DD} = 6\text{ V}, R_L = 0.1\ \Omega$ $I_D \cong 60\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$	N-Ch 2	-	7	9	
Rise Time ^c	t_r	$V_{DD} = 6\text{ V}, R_L = 0.3\ \Omega$ $I_D \cong 20\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$	N-Ch 1	-	18	23	
		$V_{DD} = 6\text{ V}, R_L = 0.1\ \Omega$ $I_D \cong 60\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$	N-Ch 2	-	17	23	
Turn-Off Delay Time ^c	$t_{d(off)}$	$V_{DD} = 6\text{ V}, R_L = 0.3\ \Omega$ $I_D \cong 20\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$	N-Ch 1	-	13	17	
		$V_{DD} = 6\text{ V}, R_L = 0.1\ \Omega$ $I_D \cong 60\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$	N-Ch 2	-	19	25	
Fall Time ^c	t_f	$V_{DD} = 6\text{ V}, R_L = 0.3\ \Omega$ $I_D \cong 20\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$	N-Ch 1	-	13	17	
		$V_{DD} = 6\text{ V}, R_L = 0.1\ \Omega$ $I_D \cong 60\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$	N-Ch 2	-	14	28	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed Current ^a	I_{SM}		N-Ch 1	-	-	80	A
			N-Ch 2	-	-	180	
Forward Voltage	V_{SD}	$I_F = 10\text{ A}, V_{GS} = 0\text{ V}$	N-Ch 1	-	0.8	1.2	V
		$I_F = 20\text{ A}, V_{GS} = 0\text{ V}$	N-Ch 2	-	0.8	1.2	

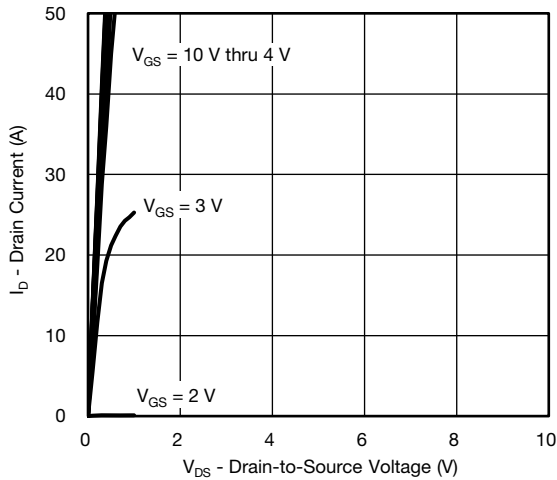
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\ \%$.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

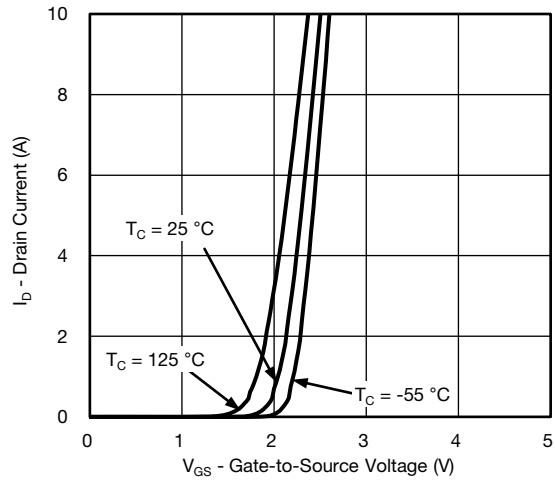
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



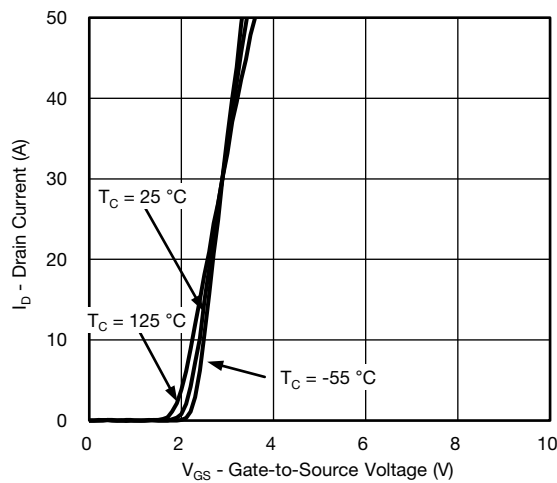
N-CHANNEL 1 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



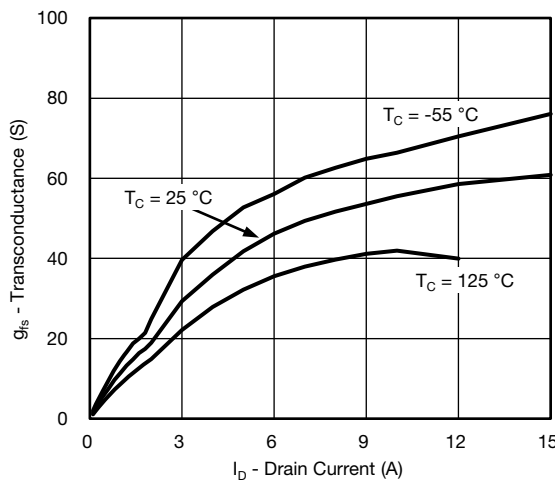
Output Characteristics



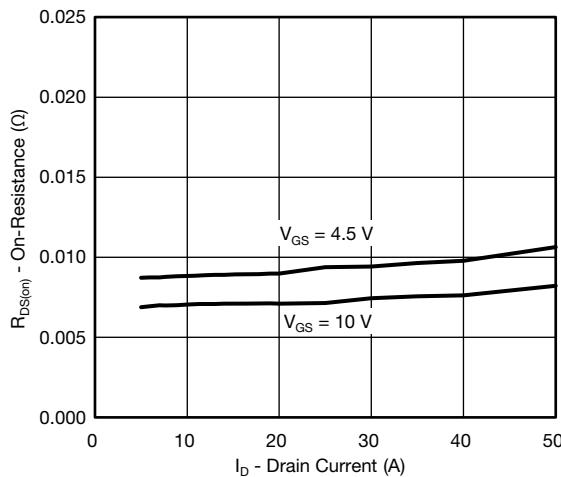
Transfer Characteristics



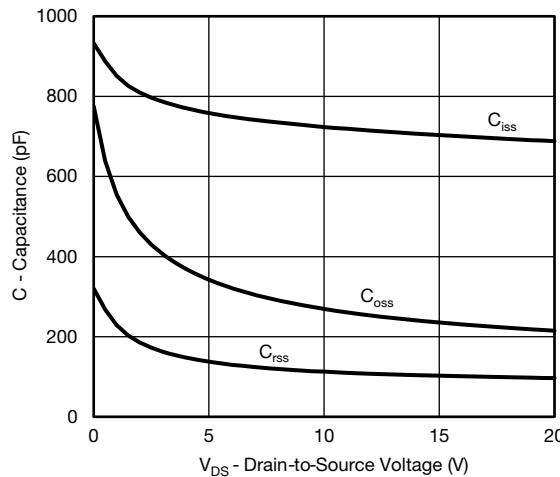
Transfer Characteristics



Transconductance



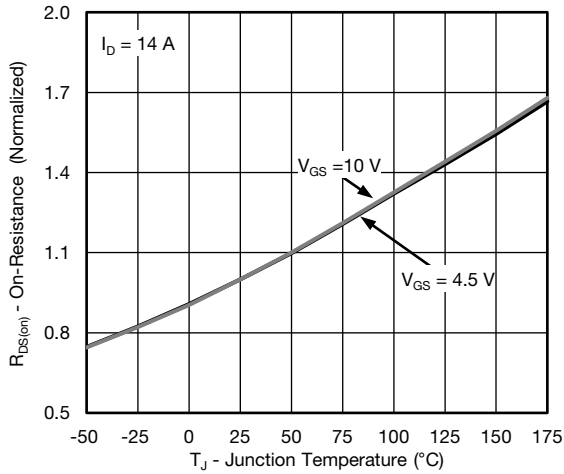
On-Resistance vs. Drain Current



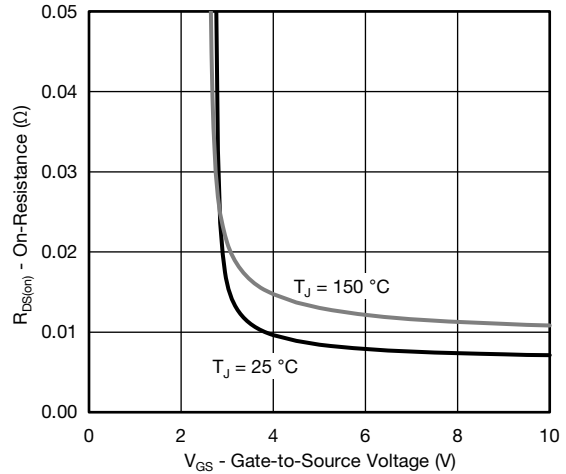
Capacitance



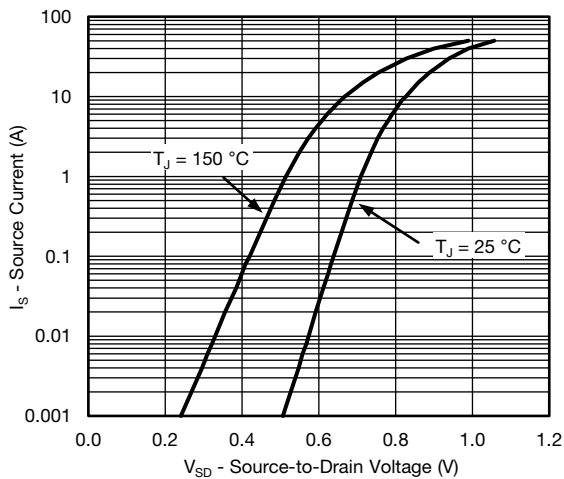
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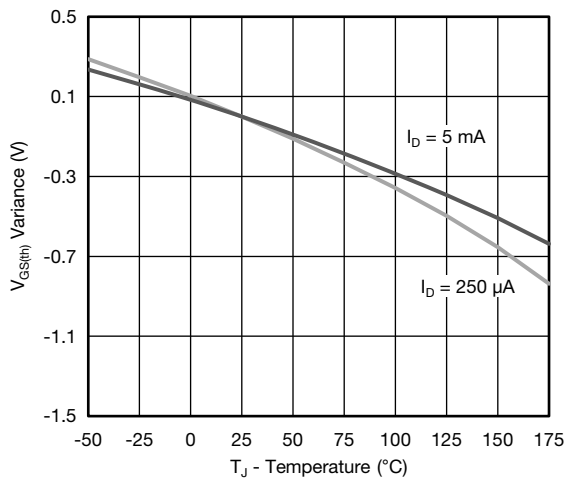
On-Resistance vs. Junction Temperature



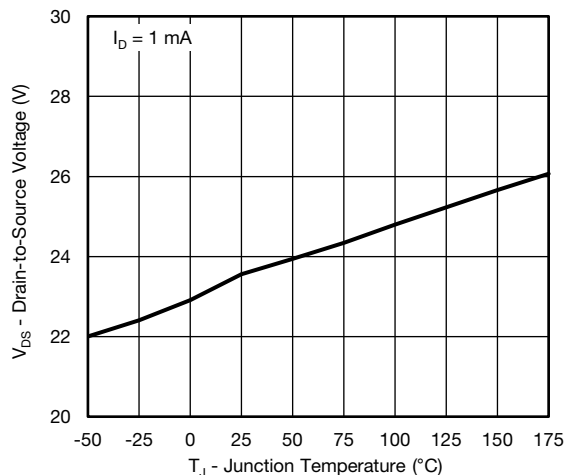
On-Resistance vs. Gate-to-Source Voltage



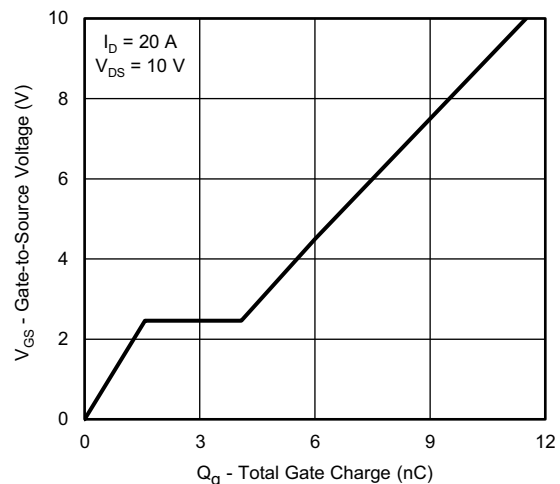
Source Drain Diode Forward Voltage



Threshold Voltage

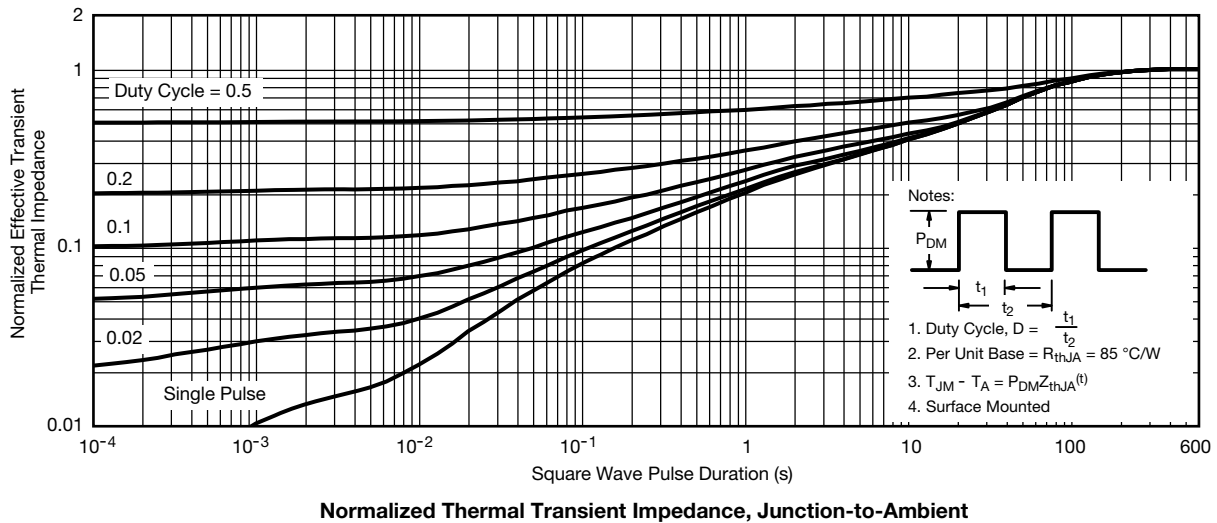
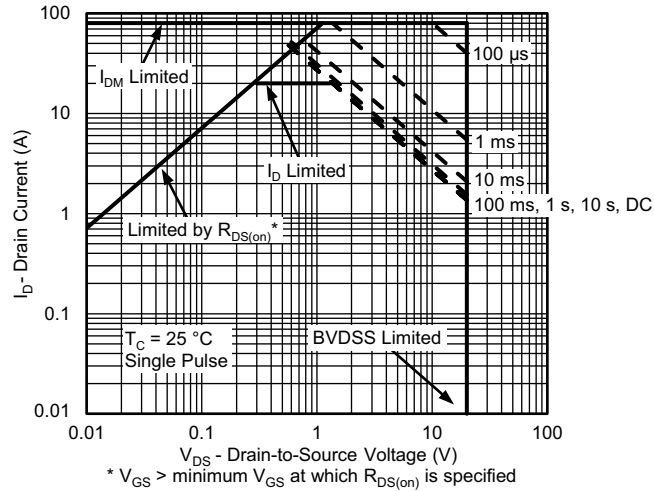


Drain Source Breakdown vs. Junction Temperature



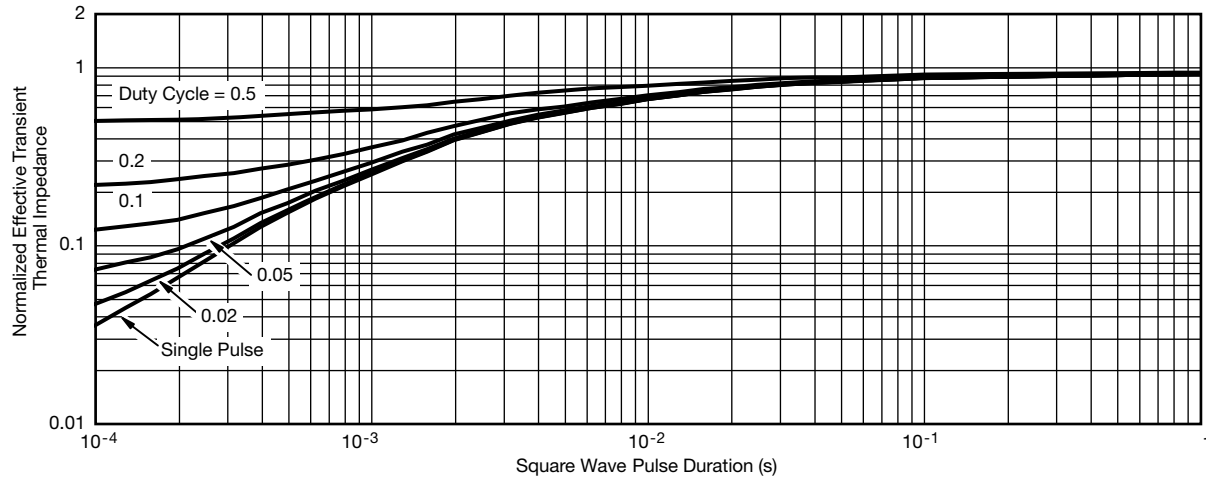
Gate Charge

N-CHANNEL 1 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)





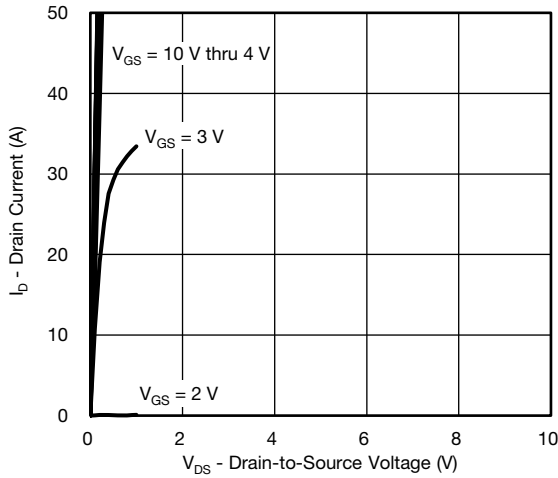
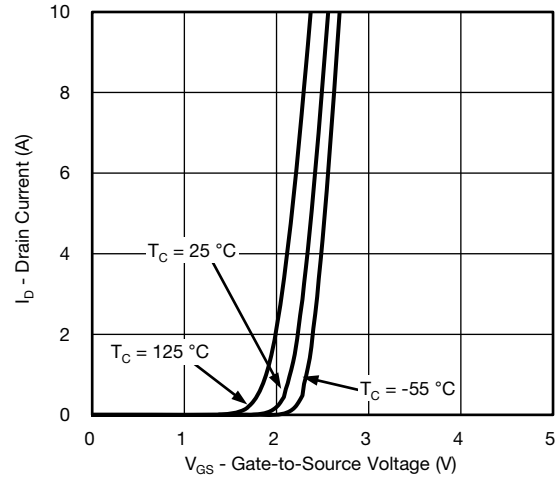
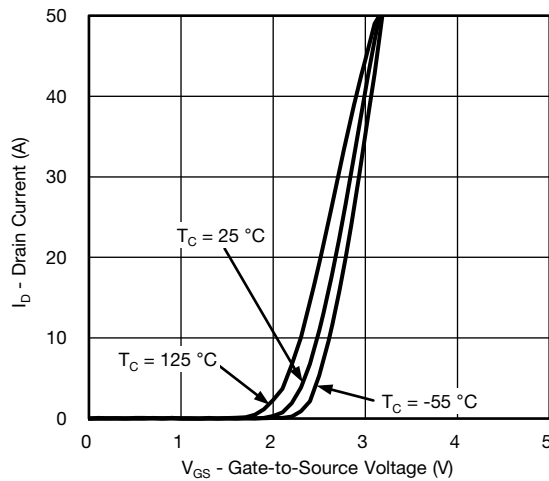
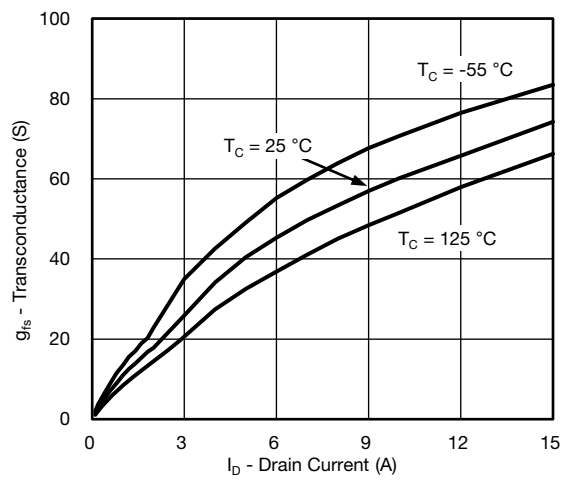
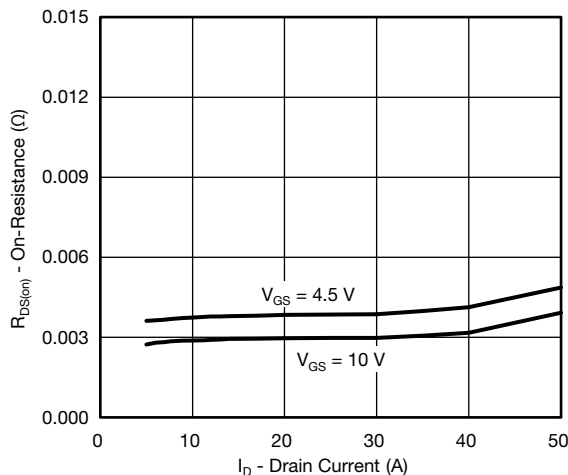
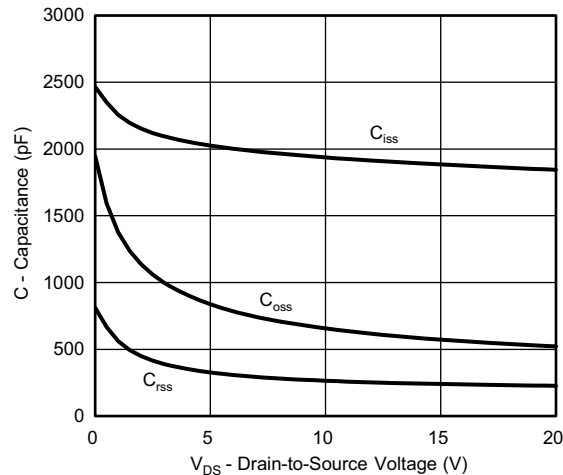
N-CHANNEL 1 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

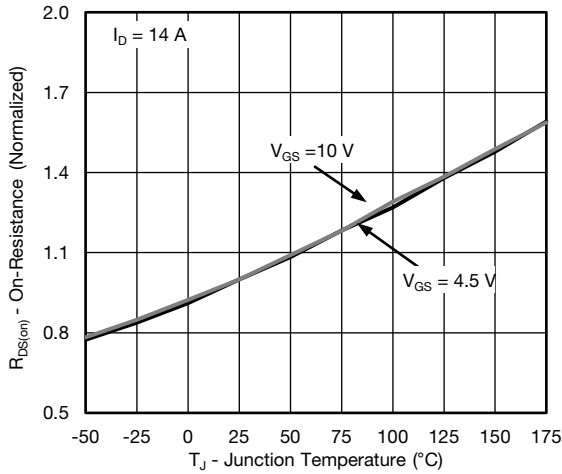
Note

- The characteristics shown in the graph:
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C) is given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

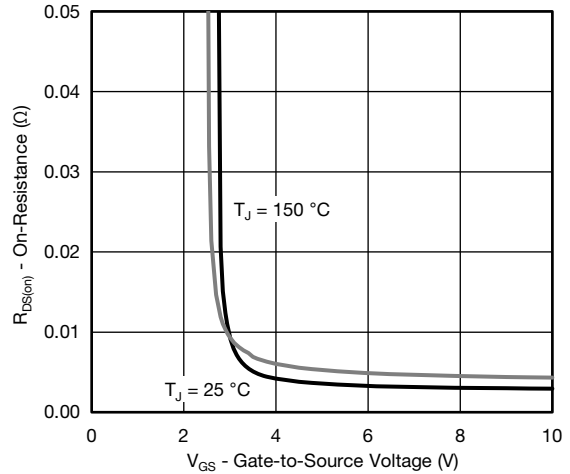
N-CHANNEL 2 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transfer Characteristics

Transconductance

On-Resistance vs. Drain Current

Capacitance



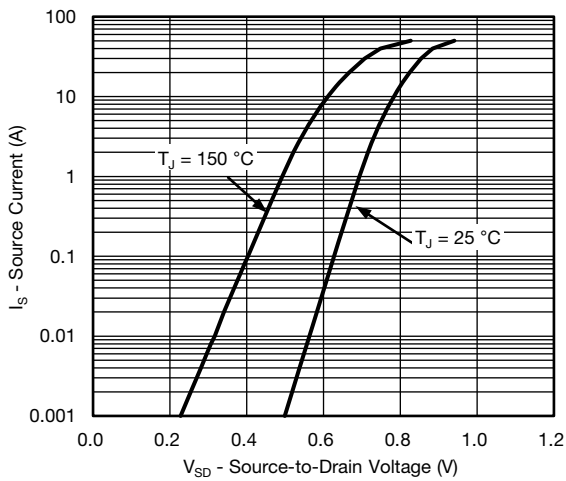
N-CHANNEL 2 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



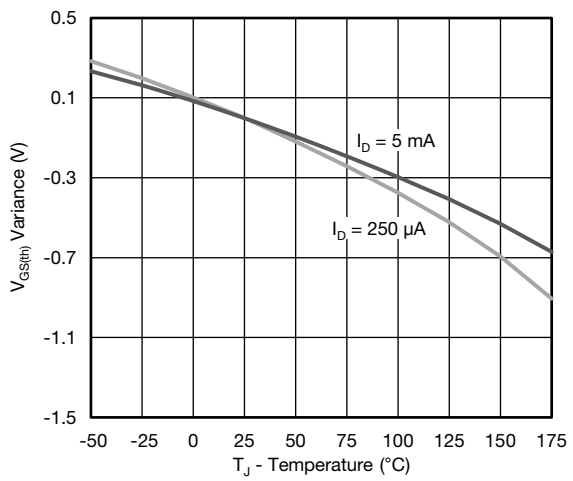
On-Resistance vs. Junction Temperature



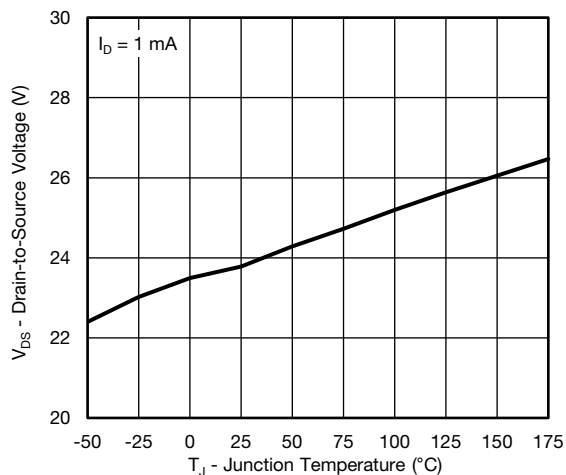
On-Resistance vs. Gate-to-Source Voltage



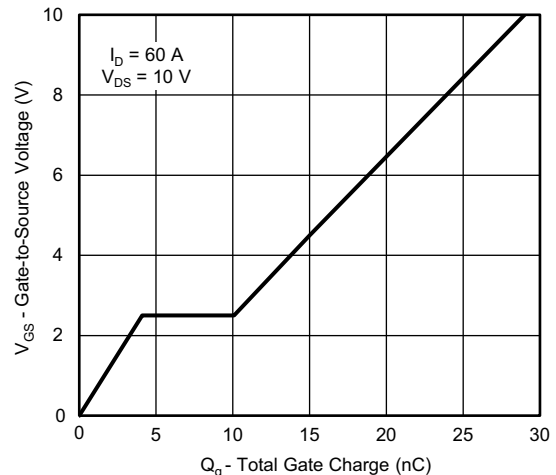
Source Drain Diode Forward Voltage



Threshold Voltage



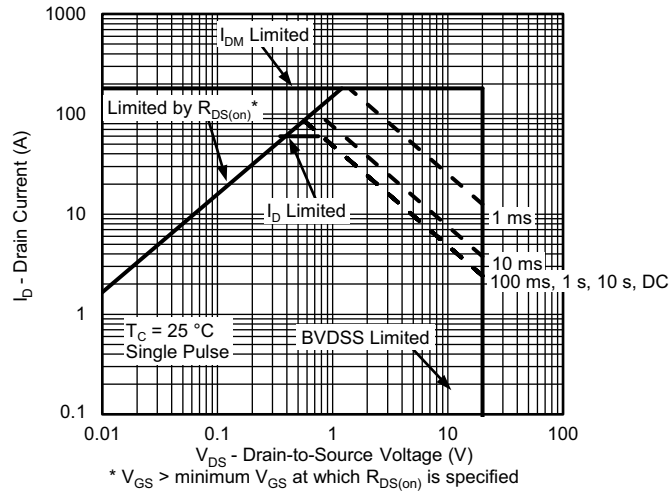
Drain Source Breakdown vs. Junction Temperature



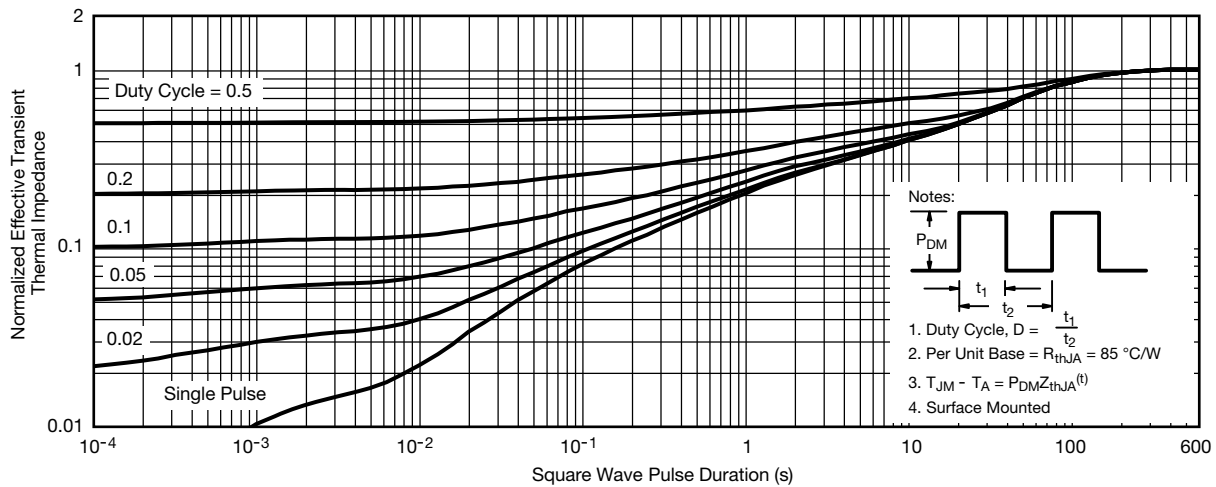
Gate Charge



N-CHANNEL 2 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



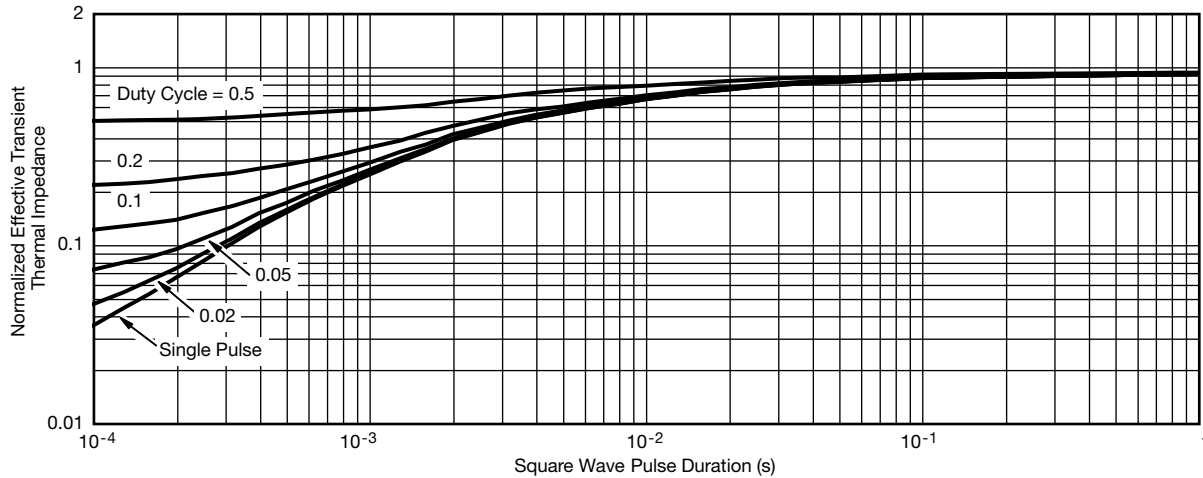
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



N-CHANNEL 2 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

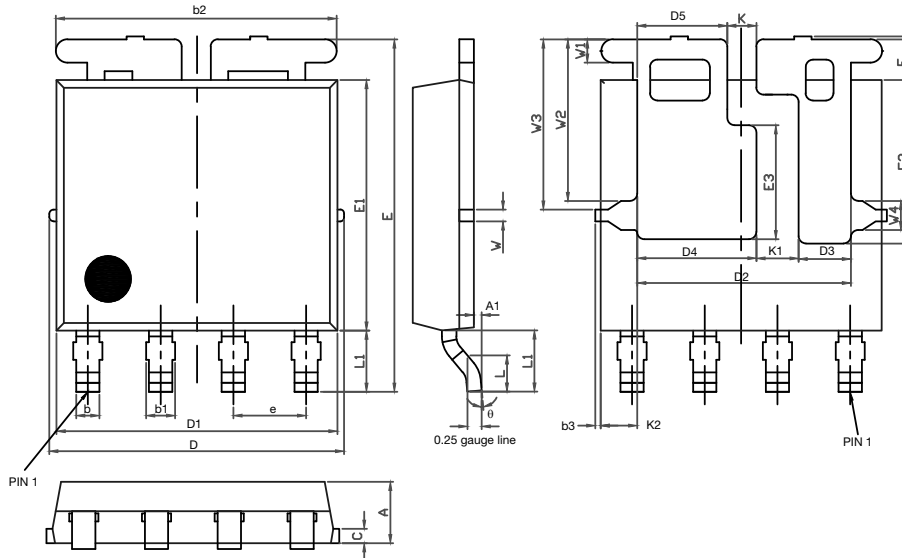
Note

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Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67774.



PowerPAK[®] SO-8L Assymmetric Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	0.06	0.13	0.000	0.003	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3	0.04	0.12	0.20	0.002	0.005	0.008
c	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.63	3.73	3.83	0.143	0.147	0.151
D3	0.81	0.91	1.01	0.032	0.036	0.040
D4	1.98	2.08	2.18	0.078	0.082	0.086
D5	1.47	1.57	1.67	0.058	0.062	0.066
e	1.20	1.27	1.34	0.047	0.050	0.053
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	2.75	2.85	2.95	0.108	0.112	0.116
E3	1.89	1.99	2.09	0.074	0.078	0.082
F	0.05	0.12	0.19	0.002	0.005	0.007
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.41	0.51	0.61	0.016	0.020	0.024
K1	0.64	0.74	0.84	0.025	0.029	0.033
K2	0.54	0.64	0.74	0.021	0.025	0.029
W	0.13	0.23	0.33	0.005	0.009	0.013
W1	0.31	0.41	0.51	0.012	0.016	0.020
W2	2.72	2.82	2.92	0.107	0.111	0.115
W3	2.86	2.96	3.06	0.113	0.117	0.120
W4	0.41	0.51	0.61	0.016	0.020	0.024
θ	5°	10°	12°	5°	10°	12°

DWG: 6009

Note

- Millimeters will govern



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