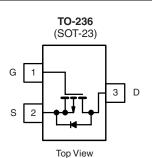


# P-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	$R_{DS(on)}\left(\Omega\right)$	I <sub>D</sub> (A) <sup>d</sup>	Q <sub>g</sub> (Typ.)			
- 60	0.345 at V <sub>GS</sub> = - 10 V	- 1.6	2.7 nC			
	0.450 at V <sub>GS</sub> = - 4.5 V	- 1.4	2.7 110			



Si2309CDS (N9)\*

\* Marking Code

Ordering Information: Si2309CDS-T1-E3 (Lead (Pb)-free)

Si2309CDS-T1-GE3 (Lead (Pb)-free and Halogen-free)

#### **FEATURES**

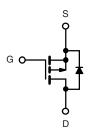
- Halogen-free Option Available
- TrenchFET® Power MOSFET



RoHS

## **APPLICATIONS**

· Load Switch



P-Channel MOSFET

Parameter		Symbol	Limit	Uni	
Drain-Source Voltage	V <sub>DS</sub>	- 60	.,		
Gate-Source Voltage		V <sub>GS</sub>	± 20		
	T <sub>C</sub> = 25 °C		- 1.6		
0 11 0 1 0 1 7 1 1 2 2 2 3 h	T <sub>C</sub> = 70 °C		- 1.3		
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a, b</sup>	T <sub>A</sub> = 25 °C	I <sub>D</sub>	- 1.2 <sup>a, b</sup>		
	T <sub>A</sub> = 70 °C		- 1.0 <sup>a, b</sup>	_	
Pulsed Drain Current (10 µs Pulse Width)		I <sub>DM</sub>	- 8	A	
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	- 5		
	T <sub>C</sub> = 25 °C	1	- 1.4		
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	- 0.9 <sup>a, b</sup>		
	T <sub>C</sub> = 25 °C		1.7		
	T <sub>C</sub> = 70 °C	В	1.1	10/	
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	1.0 <sup>a, b</sup>	W	
	T <sub>A</sub> = 70 °C		0.67 <sup>a, b</sup>		
Operating Junction and Storage Temperature Rar	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	90		
Soldering Recommendations (Peak Temperature)		260	°C		

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient <sup>a, c</sup>	t ≤ 5 s	R <sub>thJA</sub>	92	120	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	$R_{thJF}$	58	73	O/ <b>VV</b>		

#### Notes:

- a. Surface Mounted on 1" x 1" FR4 board.
- b. t = 5 s.
- c. Maximum under Steady State conditions is 166 °C/W.
- d. When  $T_C = 25$  °C.

## **Si2309CDS**

## Vishay Siliconix



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V, I}_{D} = -250 \mu\text{A}$	- 60			V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = - 250 μA		- 65		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	Ι <sub>D</sub> = - 230 μΑ		4.5		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 1		- 3	V
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			- 100	nA
Zara Cata Valtaga Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 60 V, V <sub>GS</sub> = 0 V			- 1	
Zero Gate Voltage Drain Current		V <sub>DS</sub> = - 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			- 10	μΑ
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \le 5 \text{ V}, V_{GS} = -10 \text{ V}$	- 6			Α
	_	V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 1.25 A	0.285 0.360		0.345	Ω
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 1.0 A			0.450	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = - 10 V, I <sub>D</sub> = - 1.0 A		2.8		S
Dynamic <sup>b</sup>	1			I	L	
Input Capacitance	C <sub>iss</sub>			210		pF
Output Capacitance	C <sub>oss</sub>	V <sub>DS</sub> = - 30 V, V <sub>GS</sub> = 0 V, f = 1 MHz		28		
Reverse Transfer Capacitance	C <sub>rss</sub>			20		
Total Gate Charge	Qg			2.7	4.1	nC
Gate-Source Charge	$Q_{gs}$	$V_{DS} = -30 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -1.25 \text{ A}$		0.8		
Gate-Drain Charge	$Q_{gd}$			1.2		
Gate Resistance	$R_{g}$	f = 1 MHz		7		Ω
Turn-On Delay Time	t <sub>d(on)</sub>			40	60	
Rise Time	t <sub>r</sub>	$V_{DD}$ = - 30 V, $R_L$ = 30 $\Omega$		35	55	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong$ - 1 A, $V_{GEN}$ = - 4.5 V, $R_g$ = 1 $\Omega$		15	25	
Fall Time	t <sub>f</sub>			10	20	
Turn-On Delay Time	t <sub>d(on)</sub>			5	10	ns
Rise Time	t <sub>r</sub>	$V_{DD}$ = - 30 V, $R_L$ = 30 $\Omega$		10	20	- - -
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong$ - 1 A, $V_{GEN}$ = - 10 V, $R_g$ = 1 $\Omega$		15	25	
Fall Time	t <sub>f</sub>			10	20	
<b>Drain-Source Body Diode Characteris</b>	tics					
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			- 1.4	Α
Pulse Diode Forward Current	I <sub>SM</sub>				- 8	^
Body Diode Voltage	$V_{SD}$	I <sub>S</sub> = - 0.75 A, V <sub>GS</sub> = 0 V		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	t <sub>rr</sub>		30	60	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	   I <sub>F</sub> = - 1.25 A, dl/dt = 100 A/μs, T <sub>J</sub> = 25 °C		33	60	nC
Reverse Recovery Fall Time	t <sub>a</sub>	η - 1.20 Λ, αι/αι - 100 Λ/μο, 1 J - 20 0		18		ns
Reverse Recovery Rise Time	t <sub>b</sub>	[		12		

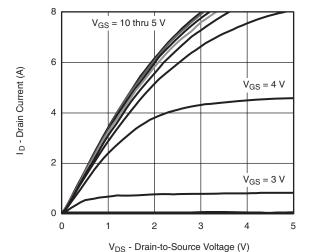
#### Notes:

- a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %.
- b. Guaranteed by design, not subject to production testing.

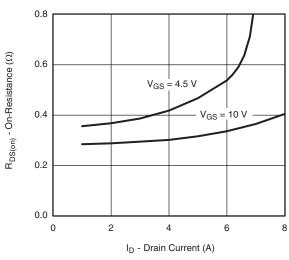
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



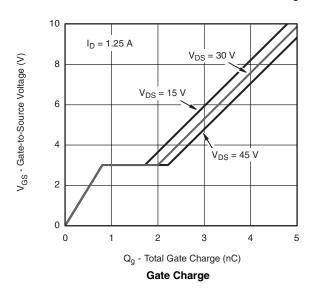
### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

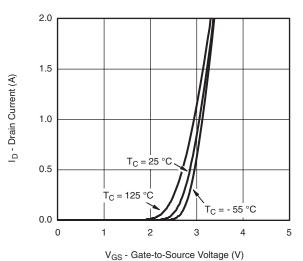


**Output Characteristics** 

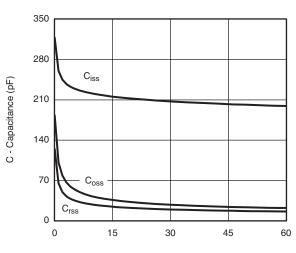


On-Resistance vs. Drain Current and Gate Voltage

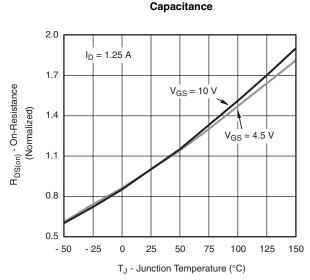




Transfer Characteristics



V<sub>DS</sub> - Drain-to-Source Voltage (V)



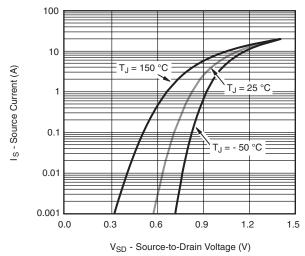
On-Resistance vs. Junction Temperature

## **Si2309CDS**

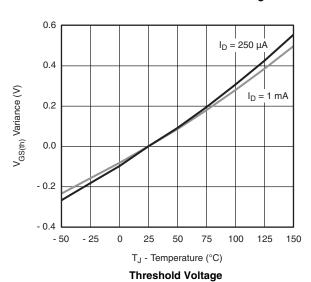
## Vishay Siliconix

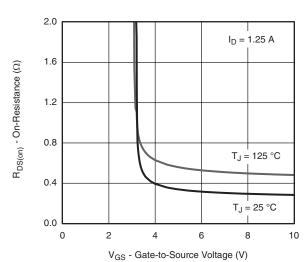
# VISHAY.

## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

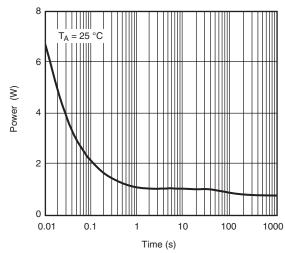


Source-Drain Diode Forward Voltage

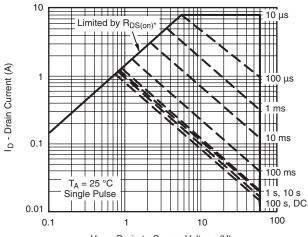




On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



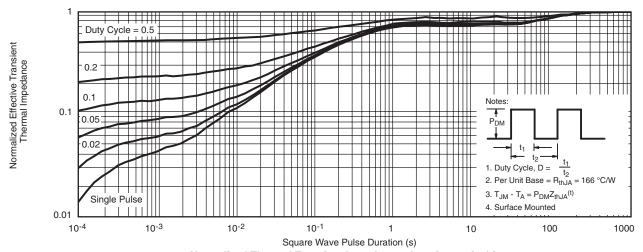
V<sub>DS</sub> - Drain-to-Source Voltage (V)

\*  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

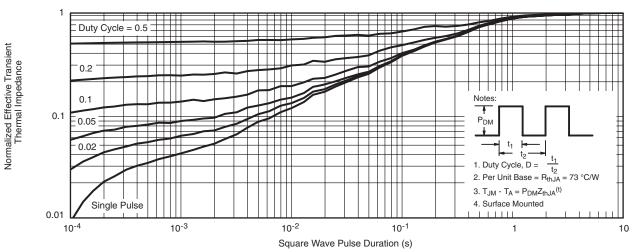
Safe Operating Area, Junction-to-Ambient



## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



#### Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="http://www.vishay.com/ppg?68980">http://www.vishay.com/ppg?68980</a>.

## SOT-23 (TO-236): 3-LEAD







Dim	MILLI	METERS	INCHES		
	Min	Max	Min	Max	
Α	0.89	1.12	0.035	0.044	
A <sub>1</sub>	0.01	0.10	0.0004	0.004	
A <sub>2</sub>	0.88	1.02	0.0346	0.040	
b	0.35	0.50	0.014	0.020	
С	0.085	0.18	0.003	0.007	
D	2.80	3.04	0.110	0.120	
E	2.10	2.64	0.083	0.104	
E <sub>1</sub>	1.20	1.40	0.047	0.055	
е	0.9	5 BSC	BSC 0.0374 R		
e <sub>1</sub>	1.9	0 BSC	0.0748 Ref		
L	0.40	0.60	0.016	0.024	
L <sub>1</sub>	0.64 Ref		0.025 Ref		
S	0.50 Ref		0.020 Ref		
q	3°	8°	3°	8°	
FCN: S-03946-Rev K 09-	lul-01	•			

ECN: S-03946-Rev. K, 09-Jul-01

DWG: 5479

Document Number: 71196 www.vishay.com 09-Jul-01



### **RECOMMENDED MINIMUM PADS FOR SOT-23**



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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