



N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY									
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A) ^a	Q _g (Typ.)						
30	0.036 at V _{GS} = 10 V	4.5							
	0.039 at V _{GS} = 4.5 V	4.5	7 nC						
	0.053 at V _{GS} = 2.5 V	4.5							

FEATURES

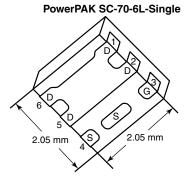
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® SC-70 Package
 - Small Footprint Area
- Compliant to RoHS Directive 2002/95/EC

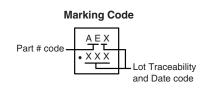


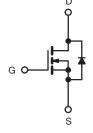
HALOGEN **FREE**

APPLICATIONS

- Load Switch for Portable Applications
- DC/DC Converter







Ordering Information: SiA408DJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

N-Channel MOSFET

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	30	V
Gate-Source Voltage		V_{GS}	± 12	v
Continuous Drain Current (T _J = 150 °C)	$T_{C} = 25 °C$ $T_{C} = 70 °C$ $T_{A} = 25 °C$ $T_{A} = 70 °C$	I _D	4.5 ^a 4.5 ^a 4.5 ^{a, b, c} 4.5 ^{b, c}	A
Pulsed Drain Current	I _{DM}	20		
Continuous Source-Drain Diode Current	$T_C = 25 ^{\circ}C$ $T_A = 25 ^{\circ}C$	Is	4.5 ^a 2.8 ^{b, c}	
Maximum Power Dissipation	$T_{C} = 25 ^{\circ}\text{C}$ $T_{C} = 70 ^{\circ}\text{C}$ $T_{A} = 25 ^{\circ}\text{C}$ $T_{A} = 70 ^{\circ}\text{C}$	P _D	17.9 11.4 3.4 ^{b, c} 2.2 ^{b, c}	W
Operating Junction and Storage Temperatur	T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Tempera	ature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS									
Parameter		Symbol	Typical	Maximum	Unit				
Maximum Junction-to-Ambient ^{b, †}	t ≤ 5 s	R_{thJA}	29	37	°C/W				
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	5.5	7					

Notes:

- a. Package limited
- b. Surface mounted on 1" x 1" FR4 board.
- d. See solder profile (www.vishay.com/ppg?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
 e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 80 °C/W.



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static	l	,		·	L	
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			٧
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	J 050 vA		30		
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	- I _D = 250 μA		- 4		mV/°C
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_{D} = 250 \mu\text{A}$	0.6		1.6	٧
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 100	nA
7 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		V _{DS} = 30 V, V _{GS} = 0 V			1	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C			10	μΑ
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			Α
	, ,	V _{GS} = 10 V, I _D = 5.3 A		0.030	0.036	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 5.1 A		0.032	0.039	Ω
		V _{GS} = 2.5 V, I _D = 2.5 A		0.040	0.053	Ī
Forward Transconductance ^a g		V _{DS} = 10 V, I _D = 5.3 A		20		S
Dynamic ^b	•			<u> </u>	L	
Input Capacitance	C _{iss}			830		
Output Capacitance	C _{oss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz		130		pF
Reverse Transfer Capacitance	C _{rss}			60		·
		V _{DS} = 15 V, V _{GS} = 10 V, I _D = 7.8 A		16	24	nC
Total Gate Charge	Q_g			7	11	
Gate-Source Charge	Q_{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 7.8 \text{ A}$		2		
Gate-Drain Charge	Q _{gd}			1.7		
Gate Resistance	R _g	f = 1 MHz	0.6	3	6	Ω
Turn-On Delay Time	t _{d(on)}			10	15	
Rise Time	t _r	$V_{DD} = 15 \text{ V, R}_1 = 2.4 \Omega$		10	15	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 6.2 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		35	55	
Fall Time	t _f			15	25	
Turn-On Delay Time	t _{d(on)}			10	15	ns
Rise Time	t _r	$V_{DD} = 15 \text{ V}, R_{L} = 2.4 \Omega$		10	15	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 6.2 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		20	30	
Fall Time	t _f	1		10	15	
Drain-Source Body Diode Characteristic	L					
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			4.5	
Pulse Diode Forward Current				1	20	A
Body Diode Voltage	V _{SD}	I _S = 6.2 A, V _{GS} = 0 V		0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}			20	40	ns
Body Diode Reverse Recovery Charge	Q _{rr}	1		15	30	nC
Reverse Recovery Fall Time	t _a	$I_F = 6.2 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		13	-	ns
Reverse Recovery Rise Time	t _b	1		7		

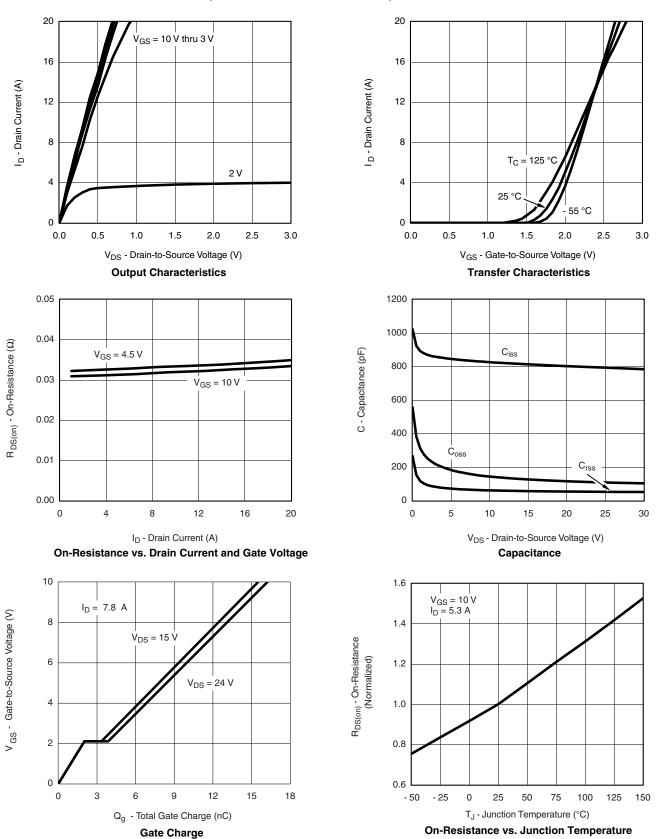
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 % b. Guaranteed by design, not subject to production testing.

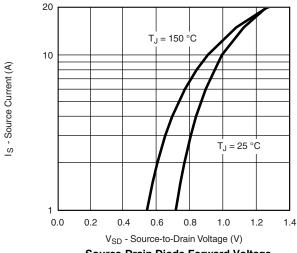




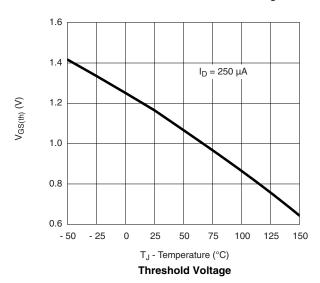
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

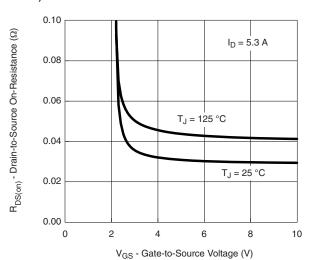


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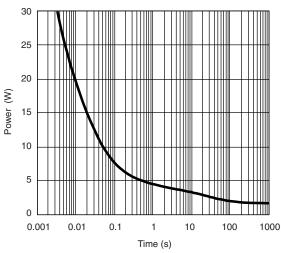


Source-Drain Diode Forward Voltage

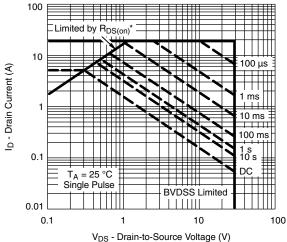




On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power (Junction-to-Ambient)



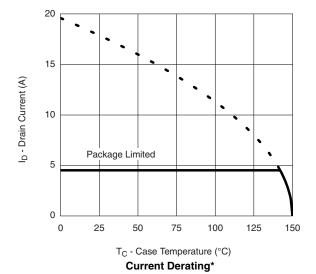
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified Safe Operating Area, Junction-to-Ambient

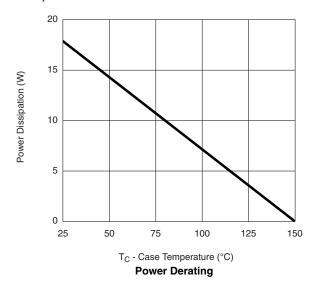






TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

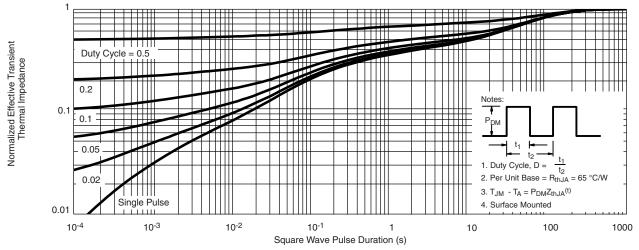




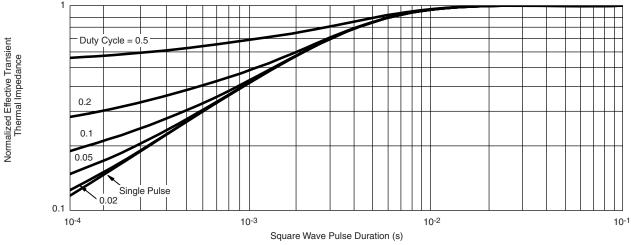
^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?69255.





PowerPAK® SC70-6L





BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



- All dimensions are in millimeters
 Package outline exclusive of mold flash and metal burr
 Package outline inclusive of plating

	SINGLE PAD						DUAL PAD						
DIM	MILLIMETERS			INCHES			MILLIMETERS			INCHES			
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
Α	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032	
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002	
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015	
С	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010	
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085	
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028	
D2	0.135	0.235	0.335	0.005	0.009	0.013							
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085	
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041	
E2	0.345	0.395	0.445	0.014	0.016	0.018							
E3	0.425	0.475	0.525	0.017	0.019	0.021							
е		0.65 BSC			0.026 BSC	;	0.65 BSC			0.026 BSC			
K		0.275 TYP			0.011 TYP		0.275 TYP		0.011 TYP				
K1		0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
K2		0.240 TYP		0.009 TYP		0.252 TYP			0.010 TYP				
К3		0.225 TYP		0.009 TYP					•	•			
K4		0.355 TYP			0.014 TYP		<u> </u>						
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015	
T							0.05	0.10	0.15	0.002	0.004	0.006	

ECN: C-07431 - Rev. C, 06-Aug-07

DWG: 5934

06-Aug-07



RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

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ATTLICATION NOT



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