Using the Single-Channel TSOP-6 As a Second-Source for the 1206-8 Single-Channel ChipFET®

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INTRODUCTION

The Vishay Siliconix ChipFET is a state-of-the-art package that evolved from the TSOP-6 format. Despite the improved power dissipation and on-resistance ratings featured in the 1206-8 ChipFET, the fact that it is currently a single-source solution is a point of concern for some customers. Vishay Siliconix designers addressed this concern by developing a common padset shared by the 1206-8 ChipFET and TSOP-6 packages, which allows for substitution in the same location on a PC board. This approach offers adequate assurance of an alternate package source.

COMPARISON

At first, the similarity between the two packages is not obvious. For 1206-8 ChipFET package dimensions visit (http://www.vishay.com/doc?71151). For TSOP-6 package dimensions visit (http://www.vishay.com/doc?71200). The ChipFET is an eight-pin, “leadless” package in which the leads are brought out from under the plastic body, while the TSOP-6 package has six leads that extend from the side. The package width also differs, with a 71-mils width for the ChipFET format as opposed to the 117-mils TSOP-6.

A closer examination shows that the plastic body size, 67 mils x 122 mils, is the same for both packages. The gate, source, and drain pin placements are also similar—in both package types, the gate and source pins are at one end of the package, with the remainder of the pins utilized as drain pins. The gate lead is located at the extreme right corner on the bottom, the source lead is at the extreme right corner on the top, and the area to the left of the gate and source leads is assigned for drain leads. This similarity in terminal orientation enables the design of a common padset that can accommodate either the ChipFET or TSOP-6 package in the same location.

COMMON FOOTPRINTS

The design of a common padset requires adherence to two criteria. The first is the alignment of each package’s gate and source leads to maintain the correct spacing for electrical isolation. The second is to utilize all of the available PC board area underneath the body of both packages for the placement of a heat-spreading copper layer. The resulting pad structure not only facilitates placement of the ChipFET or TSOP-6 package in the same location on a PC board, it also addresses the thermal efficiency of the board design.

PADSETS

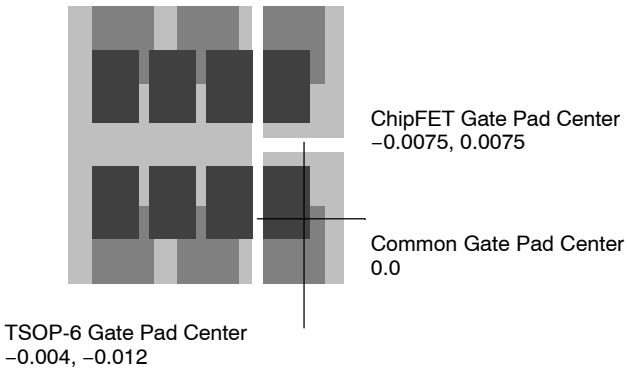


FIGURE 1. Common Padset

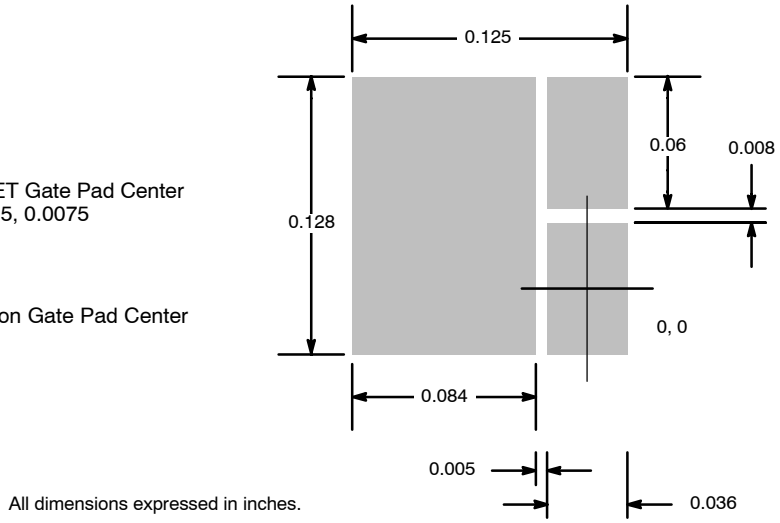


FIGURE 2. Unique Padset

To create the common padset, the basic footprint for the TSOP-6 package is placed on top of the basic footprint for the ChipFET. Refer to AN826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (http://www.vishay.com/doc?72286). This arrangement shares a horizontal centerline to achieve vertical centering. In addition, the inner left edges of the gate pads of both footprints are aligned vertically to retain the pad-to-pad spacing in the ChipFET basic footprint. Copper fill areas are then created around the gate, source, and drain pads of both packages. The outer dimensions are extended to the physical boundaries or outlines of both packages. This superimposition is shown in Figure 1, in which the offset between the two gate-pad centers is the key reference point.

The resulting padset generated by the fill areas is detailed in Figure 2.

SOLDER MASK AND STENCIL OPTIONS

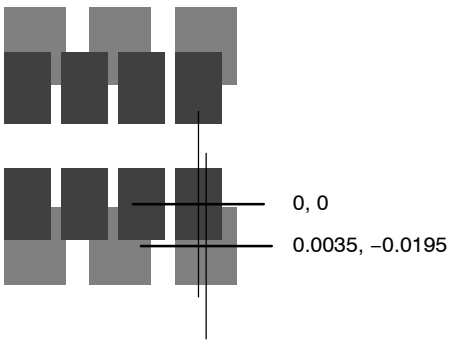
It is imperative to recognize the significance of the solder mask and the paste stencil. Large copper fills for the drain, source, and gate leads enhance the thermal capability and improve the heat removal from the MOSFET die. The part placement becomes critical on such large copper areas, however, as the part could shift dramatically and lead to assembly failure. There are two available options that address this concern. The first is to develop different solder masks and solder paste stencils for each package, enabling. the solder mask and stencil set to be changed in the middle of production to match the package being used.

The second option is to use a common solder mask that can be used with either the ChipFET or TSOP-6 package. This geometry defines a common area for the solder mask screen and generates a stencil for the application of adequate solder paste, so as to ensure good solder joints and the correct assembly.

To develop a common solder mask and stencil, the basic footprints for each package are used. The package solder masks are superimposed on top of each other as previously discussed . The superimposition shown in Figure 3 illustrates the recommended common solder mask. The offset between the two gate pad centers is useful for pick and place machines as well. Incidentally, this placement also aligns the left edge of the pad for Pin 1 of both packages.

Figure 4 illustrates the PC board implementation of the recommended common padset, which can accommodate either a 1206-8 single-channel ChipFET or a single-channel TSOP-6. The alignment between the inner left edges of the each package's gate pads—which is the key to the success of this approach—is evident in the figure. Also notice the leftward shift of the ChipFET plastic body with respect to the common padset. Conversely, the TSOP-6 plastic body is shifted to the right. The padset utilizes all of the available area underneath both packages.

The recommended common padset therefore allows the TSOP-6 package to be used as an alternative for the 1206-8 ChipFET, adequately addressing customers' concerns about availability while introducing ChipFET 1206-8 as a state-of-the-art solution.



All dimensions expressed in inches.

FIGURE 3. Common Solder Mask

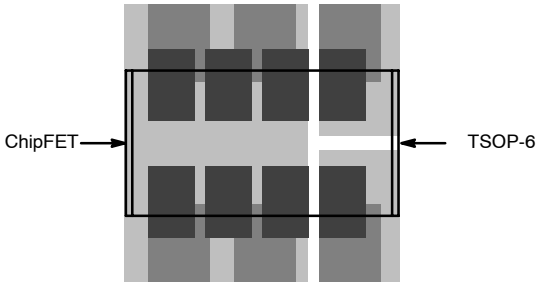


FIGURE 4. PC Board Implementation