"PowerPAK 1212-8", The Proven Automotive Package

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INTRODUCTION

This application note presents useful information on the PowerPAK 1212-8 to facilitate SQE and design engineers.

Vishay introduced the PowerPAK power MOSFET package family in the late 1990s to provide a thermally efficient solution for the computer and telecom markets. PowerPAK's combination of a small form factor and high power handling capabilities quickly brought industry-wide acceptance in various applications such as dc-to-dc power supplies, point of load, and control actuators. In most such applications, the PowerPAK SO-8 and often the PowerPAK 1212-8 can replace the much larger and bulkier DPAK.

The automotive industry embraces a new package type only after a track record has been established and extensive testing has been carried out both by manufacturers and systems engineers. The PowerPAK 1212-8 has undoubtedly won the industry's acceptance and has been successfully tested for AEC-Q101 compliance. The package has also successfully been tested on a 16-layer PC board assembly for solder joint reliability, passing the temperature cycles, including the re-work, as per IPC 9701 test guidelines.

Automotive designers have ventured to use the PowerPAK 1212-8 in such crucial applications as engine control units (ECU) and fuel injection systems. These applications demand power cycling and some UIS capabilities. PowerPAK's reliability has likewise encouraged designers to use the PowerPAK 1212-8 to replace die-level implementations, thereby eliminating the associated assembly costs while utilizing well established reflow processes. As of April 2010, more than 5.5 million PowerPAK power MOSFETs had been shipped to Vishay automotive customers worldwide.

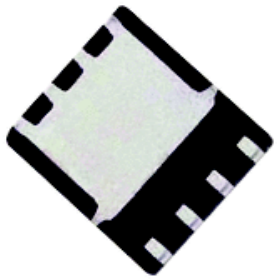

Fig. 1 - PowerPAK 1212-8 Single

Fig. 2 - PowerPAK 1212-8 Single and Dual

TABLE 1 - PACKAGE COMPARISON

PACKAGE	DIMENSION (mm)	PCB AREA (mm^2)	COMPARABLE PART POWER RATING (W)
PowerPAK 1212-8	3.4 x 3.4 x 1.12	11.56	1.5
SOIC-8	5.0 x 4.0 x 1.75	20	1.7
DPAK	10.41 x 6.73 x 2.38	70.06	2.0

APPLICATION NOTE

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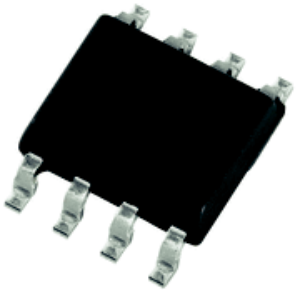

Fig. 3 - SOIC-8

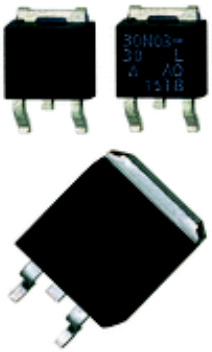

Fig. 4 - DPAK

RECOMMENDED MINIMUM PADS

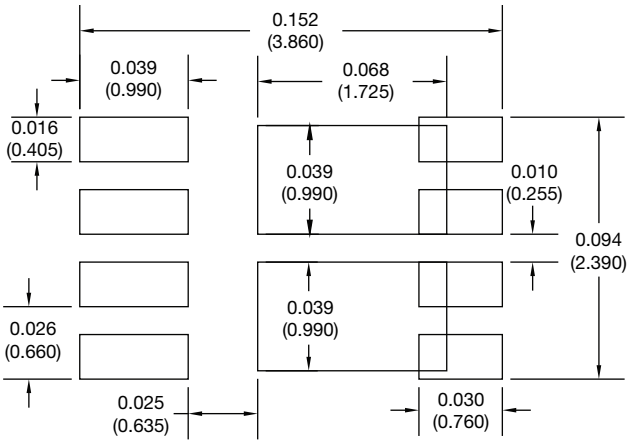

Fig. 5 - PowerPAK 1212-8 Dual

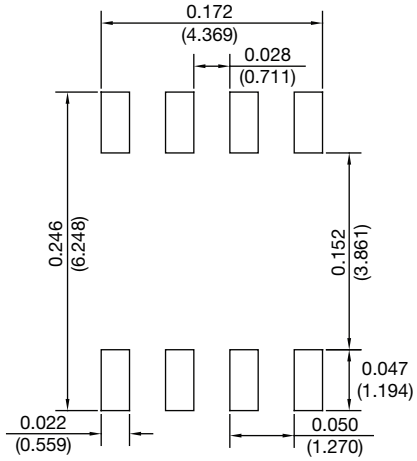

Fig. 6 - SOIC-8

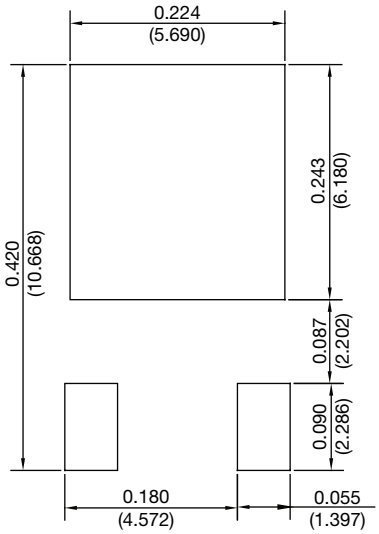

Fig. 7 - DPAK (TO-252)

AEC-Q101 COMPLIANCE FOR AUTOMOTIVE APPLICATIONS

The power temperature cycling test specified by Automotive Electronic Council document AEC Q101 for discrete components is one of the most crucial tests for automotive applications. The test requires temperature cycling of the die with a delta of 100 °C by means of active power dissipation in the die. This process puts severe thermal stresses on the package from the inside out. The solder joints on the PCB assembly must also sustain the thermal stress. PowerPAK 1212-8 was designed to address both these aspects of thermal stress and has thus achieved AEC Q101 qualification as well as passing further DV/PV tests at the automotive electronics design center. The AEC-Q101 qualification test definitions are given in the

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following table:

AEC - Q101 - REV - C
June 29, 2005

Automotive Electronics Council
Component Technical Committee

TABLE 2 - QUALIFICATION TEST DEFINITIONS

#	STRESS	ABRV	DATA TYPE	NOTE	SAMPLE SIZE PER LOT	# OF LOTS	ACCEPT ON # FAILED	REFERENCE (CURRENT REVISION	ADDITIONAL REQUIREMENTS
10	Intermittent Operational Life	IOL	1	DGTU WP	77	1 Note B	0	MIL-STD-750 Method 1037	Tested per duration indicated in Timing Requirements table on Page 13. T_A = 25 °C. Devices powered to insure $\Delta T_J \geq 100$ °C (not to exceed absolute maximum ratings). Test before and after IOL as a minimum.
10 alt	Power and Temperature Cycle	PTC	1	DGTU W	77	1 Note B	0	JESD22 A-105	Perform PTC if $\Delta T_J \geq 100$ °C cannot be achieved with IOL. Tested per duration indicated for Timing Requirements in Table 2A. Devices powered and chamber cycled to insure $\Delta T_J \geq 100$ °C (not to exceed absolute maximum ratings). Test before and after PTC as a minimum.

TABLE 2A - INTERMITTENT OPERATIONAL LIFE (TEST 10) OR POWER TEMP CYCLING (ITEM 10ALT) TIMING REQUIREMENTS

PACKAGE TYPE	NUMBER OF CYCLES REQUIRED $\Delta T_J \geq 100$ °C	NUMBER OF CYCLES REQUIRED $\Delta T_J \geq 125$ °C	TIME PER CYCLE
Small (e.g. SMD SOTS thru DPAK, and all LEDs)	15 000	7500	2 min. on/2 min. off
Medium (e.g. TO-220, D^2PAK)	8572	4286	3.5 min. on/3.5 min. off
Large (e.g. TO-3, TO-247)	6000	3000	5 min. on/5 min. off
Leadless Not to exceed:	60 000/(x+y) 15 000 cycles	30 000/(x+y) 7500 cycles	Fastest capable (minimum 2min. on/off) x min. on + y min. off

Note

- Example 1: A package capable of 2 min. on/4 min. off would require 10 000 cycles [60 000/(2 + 4)] at $\Delta T_J \geq 100$ °C or 5000 cycles at $\Delta T_J \geq 125$ °C
- Example 2: A package capable of 1 min. on/1 min. off would require 15 000 cycles at $\Delta T_J \geq 100$ °C or 7500 cycles at $\Delta T_J \geq 125$ °C

All Vishay Siliconix automotive grade, AEC-Q101 qualified power MOSFETs are numbered with an SQ prefix, i.e. SQxxx.

SOLDER JOINT RELIABILITY ON FR4 PC BOARDS

The PowerPAK 1212-8 is qualified for Solder Joint Reliability based on the guidelines stated in IPC 9701. Two separate DOEs were conducted with different third-party vendors for PC board assembly and temperature cycle testing.

The first DOE employed simple double-sided. 2-layer FR4 PCB measuring 50 mm x 50 mm x 1.5 mm with 0.076 mm (2 oz.) copper on both sides. A detailed test description is covered in application note AN825 "The Solderability of the PowerPAK SO-8 and PowerPAK 1212-8 when using different solder paste and reflow profiles," web link: http://www.vishay.com/docs/72116/72116.pdf.

The second DOE used a16-layer FR4 PC board with dimensions of 130 mm x 115 mm x 3.175 mm. Refer to figure 8. This considerable thermal mass subjects the solder joint to considerably severe stress during temperature cycling. Such a PCB design thus covers most of the extreme applications. The layer stack comprised two outer copper layers of 35 µm (1.0 oz.) and 14 inner copper layers of 12 µm (0.5 oz.). Each insulation layer of the FR-4 in between is 231 µm (7709 µin.). Appendix A covers the PCB specifications. For this experiment, an immersion silver board finish was used as per recommendations from external contract manufacturers.

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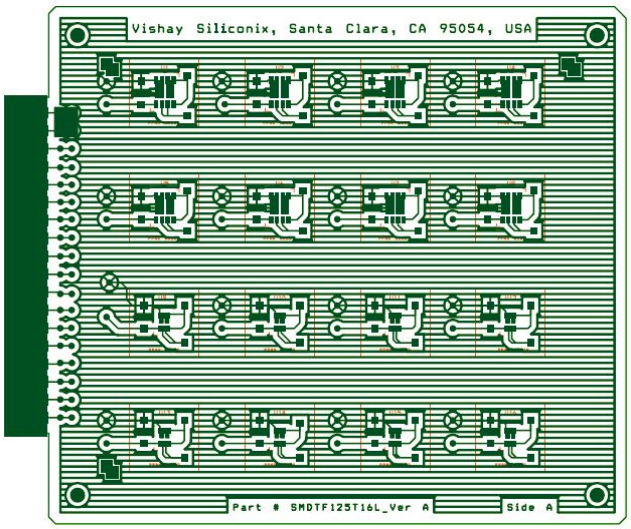

Fig. 8 - FR4 16-layer PCB

Overview of Assembly Process

(1) Lead (Pb)-free and tin-lead solder paste test samples were used:

a. Lead (Pb)-free solder paste SAC-387 (Tamura TLF-206-93G)

b. Tin-lead (Sn-Pb) no-clean solder paste Sn63-Pb37 (Alpha Metal UP78)

(2) A suitable lead (Pb)-free reflow assembly process was developed by multiple experiments involving different parameters such as aperture, stencil thickness, solder paste printing pressure. Also various solder pastes were experimented with to determine suitability of a paste.

(3) In addition, a control lot was employed using regular parts and tin-lead (Sn-Pb) solder paste. The latter establishes a base line for comparison.

IPC 9710 GUIDELINES FOR TEMPERATURE CYCLING TEST FOR SOLDER JOINT RELIABILITY

Sample size: 42 pieces of PowerPAK 1212-8 dual

Test vehicle: PCB designed to connect each pin of a part in a daisy chain and terminated on end connector to facilitate monitoring the daisy chain for each part on an automatic scanner. The PCB design also facilitates isolating each part and remove from the PCB assembly for further analysis, without disturbing the remaining parts' daisy chains. Refer to figure 9.

This DOE involves the part modifications: (a) Dies are dummy - no electrical connections. (b) Place internal bond wire jumpers - shown dotted blue lines - between two consecutive pins in pairs. The later in conjunction with the PCB layout facilitates a single daisy chain connection for each part. Refer to figure 10.

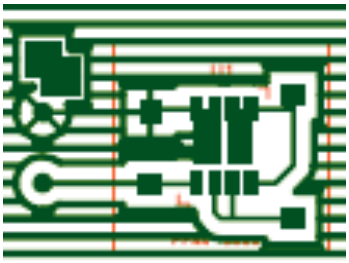

Fig. 9 - Daisy Chain Layout

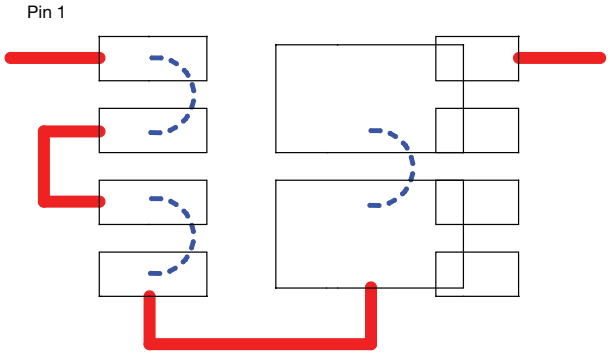

Fig. 10 - Component Modification for Daisy Chain Connection

Evenly distribute the samples on 6 PC board. Each PCB consisted of seven PowerPAK 1212-8 dual parts. Thus the 8th loaction on the PBC is unused. Identify and re-work last two parts from the first five PC boards. Total 10 re-worked parts.

Re-Work Steps

- Removing existing part using hot air BGA re-work station (laboratory setup)
- Clean up pads using soldering iron and de-soldering wick
- Solder bump pads using a soldering iron and solder wire SAC 305
- Apply no clean gel flux on pads
- Place fresh component using hot air BGA rework station
- Solder the component using hot-air BGA rework station using reflow profile shown in figure 12

DOE Reflow Process Development

The goal here is to develop/define a reflow process that can maintain the solder void level = < 20 %. The key variables are solder paste and stencil design - aspect ratio, aperture opening, machine parameters such as solder paste printing speed, pressure etc. All this eventually turns into in-house expertise of the assembly house/contract manufacturers. 2DX and if necessary 5DX x-ray results help narrow down

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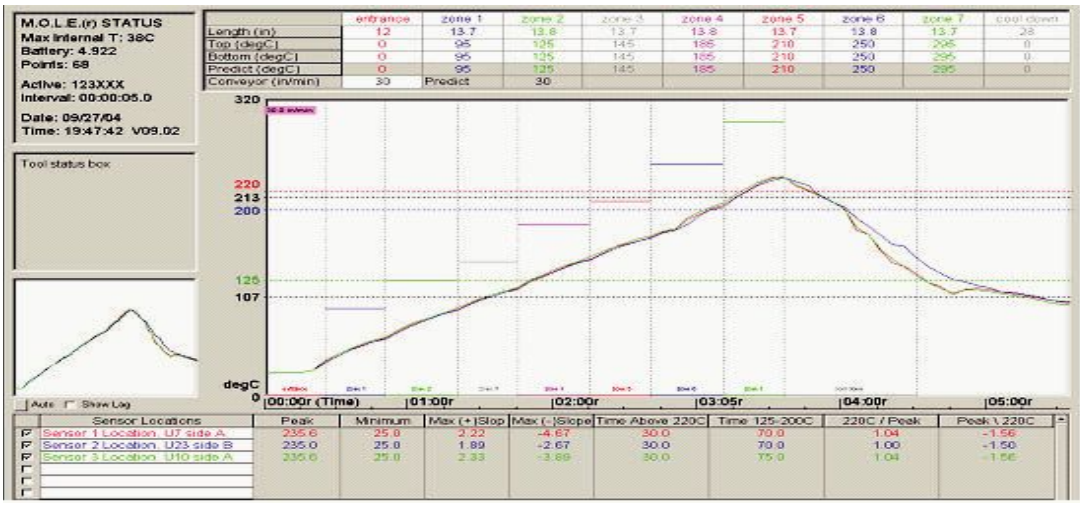
the solder paste selection and profile tweaking.

Equipment and Material

- EKRA E5 solder paste printer
- Juki E2060 pick and place machine
- BTU Pyramax 98 reflow oven
- Agilent 5DX Series 5300 laminography X-ray
- Nicolet NXR-1400 transmission X-ray
- 30x microscope
- Lead (Pb)-free solder paste SAC-387 (Tamura TLF-206-93G)
- Tin-lead (Sn-Pb) no-clean solder paste Sn63-Pb37 (Alpha Metal UP78)
- 4-mil and 5-mil stencils with a variety of aperture and aspect ratios
- Vishay PowerPAK components
- Vishay Siliconix PCB version SMD125T16L_Ver C Side A

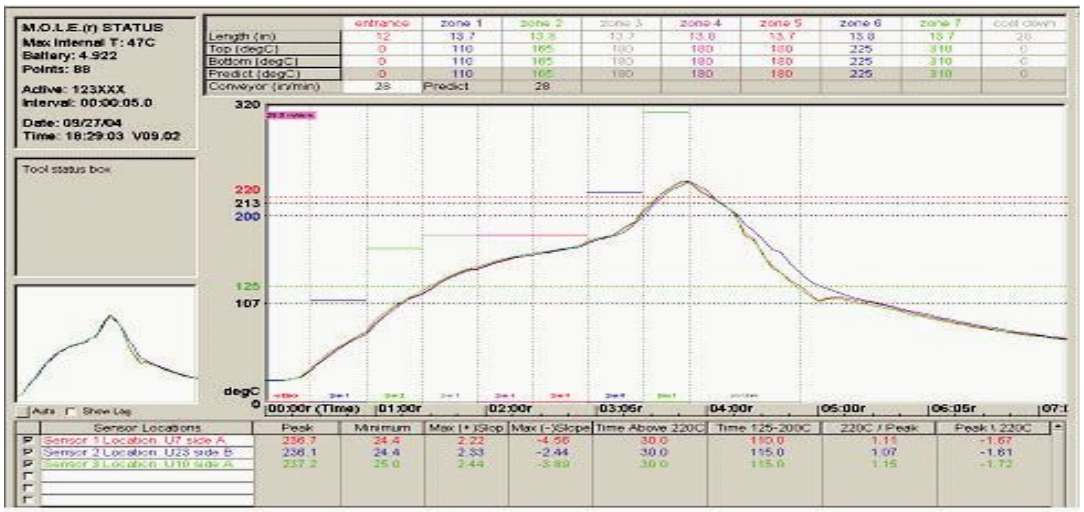
Reflow Profile Definitions

- Ramp-to-spike: RTS, figure 11
- Ramp-soak-spike: Reg RSS, figure 12
- Ramp-long-soak-spike: Long RSS, figure 13
- Ramp-soak-spike: Reg RSS for tin-lead (Sn63/Pb37) solder paste, figure 14



Peak temp. 235 °C
Time above 220 °C: 30 s
Soak time (120 °C to 200 °C): 70 s

Fig. 11 - RTS Profile for Lead (Pb)-free Solder Paste



Peak temp. 237 °C
Time above 220 °C: 30 s

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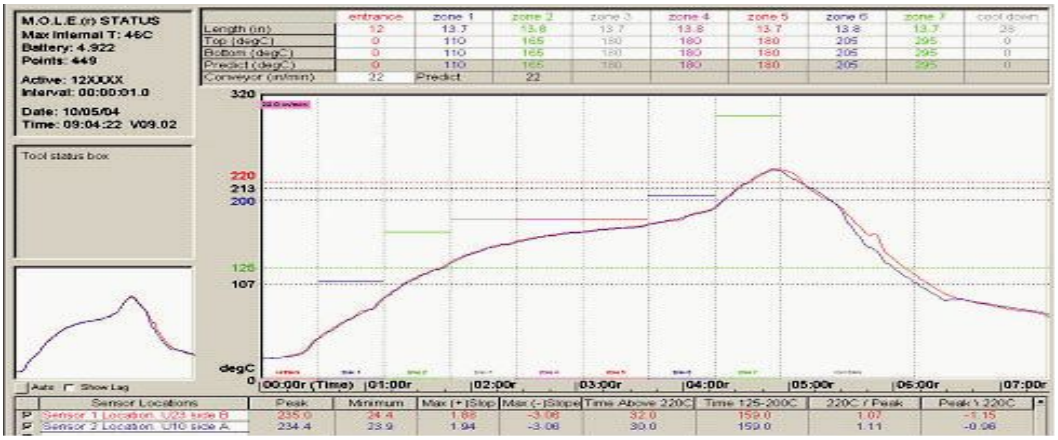
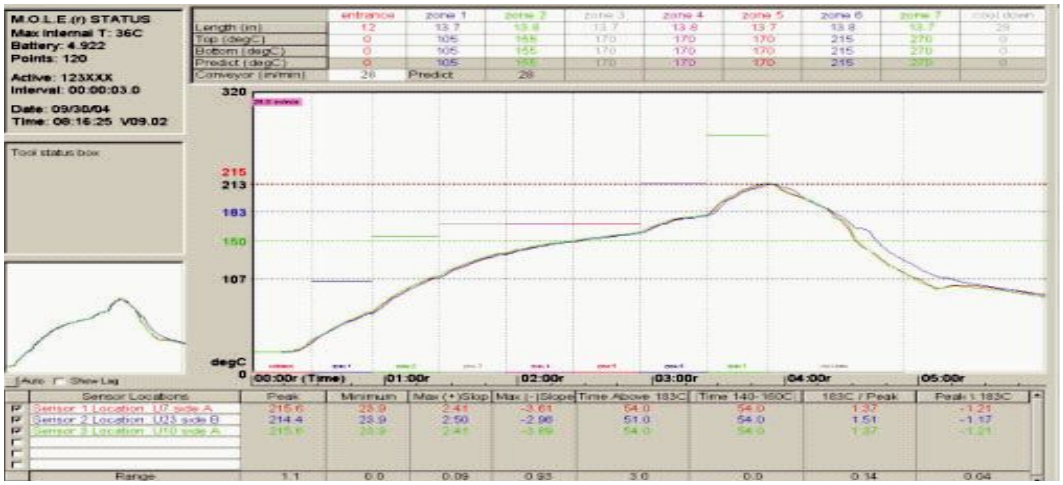
Fig. 12 - RSS Profile for Lead (Pb)-free Solder Paste



Peak temp. 235 °C
Time above 220 °C: 30 s
Soak time (120 °C to 200 °C): 159 s

Fig. 13 - LRSS Profile for Lead (Pb)-free Solder Paste



Peak temp. 215 °C
Time above 183 °C: 54 s
Soak time (140 °C to 160 °C): 54 s

Fig. 14 - RSS Profile for Tin Lead (Sn63/Pb37) Solder Paste

TABLE 3 - ASSEMBLY PARAMETERS

VERSION	COMP TYPE	BUILD QTY	PROFILE	STENCIL THICKNESS	APERTURE DESIGN	
					SIGNAL (MILS)	GROUND
AA	PowerPAK 1212D	7	RSS	4 mils	16.8 x 44	Equal to Comp.

APPLICATION NOTE

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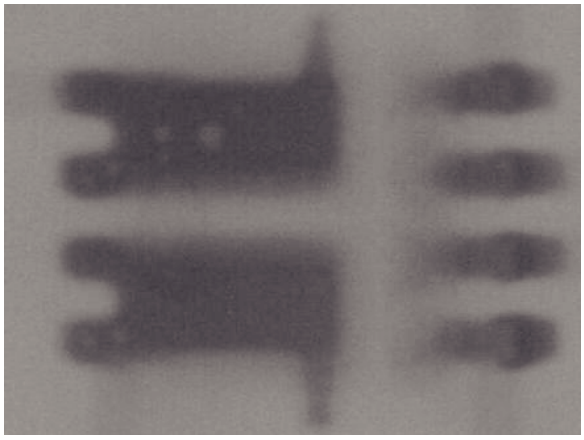


Fig. 15 - Best Case Soldering

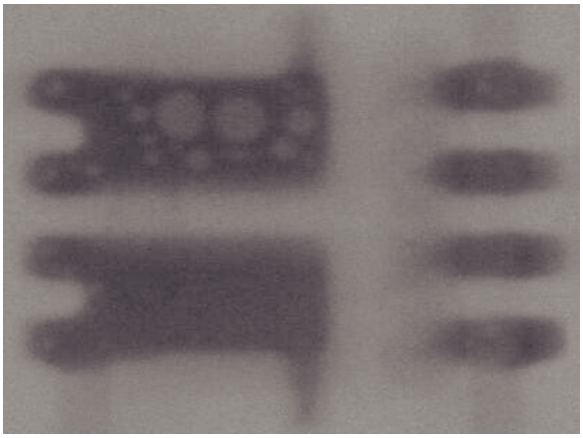


Fig. 16 - Worst Case Soldering

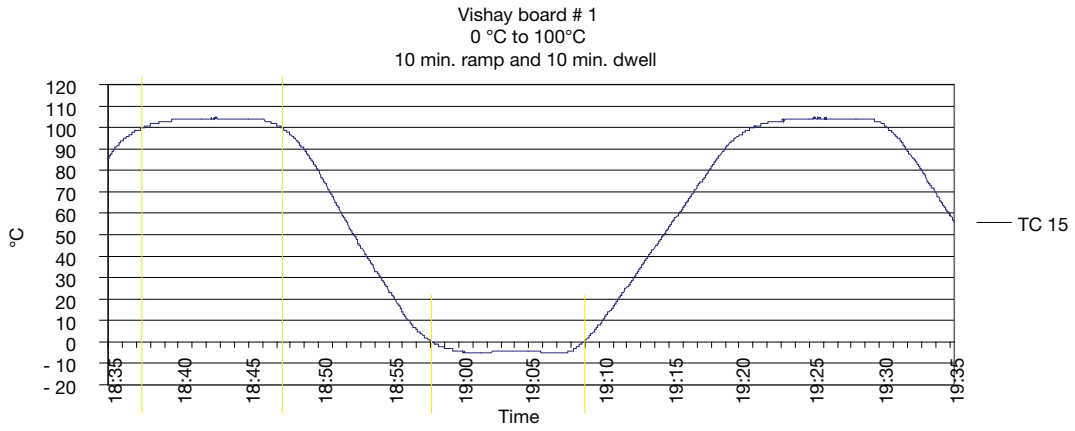
Conclusions and Recommendations of the DOE

- The minimum acceptable aspect ratio (smallest aperture opening/stencil thickness) is 2.5
- The minimum acceptable area ratio (LxW / 2(L + W)T) is 0.8
- The RSS profile shown in figure 12 is recommended for lead (Pb)-free solder paste
- The RSS profile shown in figure 14 is recommended for tin-lead solder paste

PHASE II SOLDER JOINT RELIABILITY STUDY

Temperature Cycling

- 3000 cycles of 0 °C to 100 °C temp. cycling with event recording for Daisy-Chain solder joint



Vishay PCB A
IPC9701
Cycling
0/100 40 min
cycle

Solderability Data

- Status
- 3000 Temp. cycles completed
- Statistics

PACKAGE	FIRST FAIL	# FAILED	% FAILED	SOLDER
PPAK 1212D		0	0%	Lead-free

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SLOT #	BOARD #	PACKAGE	PCB DES.	PCB SIDE	SITE ID	NET #	FAIL CYCLE
7	1	PowerPAK 1212D	A	Front	U1	97	
7	1	PowerPAK 1212D	A	Front	U2	98	
7	1	PowerPAK 1212D	A	Front	U3	99	
7	1	PowerPAK 1212D	A	Front	U4	100	
7	1	PowerPAK 1212D	A	Front	U5	101	
7	1	PowerPAK 1212D	A	Front	U6	102	
7	1	PowerPAK 1212D	A	Front	U7	103	
7	1	N/A	A	Front	U8	104	N/A
8	2	PowerPAK 1212D	A	Front	U1	113	
8	2	PowerPAK 1212D	A	Front	U2	114	
8	2	PowerPAK 1212D	A	Front	U3	115	
8	2	PowerPAK 1212D	A	Front	U4	116	
8	2	PowerPAK 1212D	A	Front	U5	117	
8	2	PowerPAK 1212D	A	Front	U6	118	
8	2	PowerPAK 1212D	A	Front	U7	119	
8	2	N/A	A	Front	U8	120	N/A
9	3	PowerPAK 1212D	A	Front	U1	129	
9	3	PowerPAK 1212D	A	Front	U2	130	
9	3	PowerPAK 1212D	A	Front	U3	131	
9	3	PowerPAK 1212D	A	Front	U4	132	
9	3	PowerPAK 1212D	A	Front	U5	133	
9	3	PowerPAK 1212D	A	Front	U6	134	
9	3	PowerPAK 1212D	A	Front	U7	135	
9	3	N/A	A	Front	U8	136	N/A
10	4	PowerPAK 1212D	A	Front	U1	145	
10	4	PowerPAK 1212D	A	Front	U2	146	
10	4	PowerPAK 1212D	A	Front	U3	147	
10	4	PowerPAK 1212D	A	Front	U4	148	
10	4	PowerPAK 1212D	A	Front	U5	149	
10	4	PowerPAK 1212D	A	Front	U6	150	
10	4	PowerPAK 1212D	A	Front	U7	151	
10	4	N/A	A	Front	U8	152	N/A
11	5	PowerPAK 1212D	A	Front	U1	161	
11	5	PowerPAK 1212D	A	Front	U2	162	
11	5	PowerPAK 1212D	A	Front	U3	163	
11	5	PowerPAK 1212D	A	Front	U4	164	
11	5	PowerPAK 1212D	A	Front	U5	165	
11	5	PowerPAK 1212D	A	Front	U6	166	
11	5	PowerPAK 1212D	A	Front	U7	167	
11	5	N/A	A	Front	U8	168	N/A
12	6	PowerPAK 1212D	A	Front	U1	177	
12	6	PowerPAK 1212D	A	Front	U2	178	
12	6	PowerPAK 1212D	A	Front	U3	179	
12	6	PowerPAK 1212D	A	Front	U4	180	
12	6	PowerPAK 1212D	A	Front	U5	181	
12	6	PowerPAK 1212D	A	Front	U6	182	
12	6	PowerPAK 1212D	A	Front	U7	183	
12	6	N/A	A	Front	U8	184	N/A

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Summary

- PowerPAK 1212 can replace the SOIC-8 and DPAK in applications requiring power dissipation up to 1.5 W.
- AEC-Q101 qualification proves the ruggedness demanded by automotive applications.
- IPC-9701 qualification establishes solderability, both for the simple two-layer PCB described in the application note AN825 and in the toughest board design described in the DOE above.
- The purpose of the DOE is to exemplify a successful assembly for a given PCB board assembly and manufacturing process. However, these simple guidelines can be used for developing the pad designs, solder profiles, aperture design and other manufacturing process parameters for successful reflow assembly of PowerPAK 1212-8 package in other PC board designs. However, we should note that each individual assembly may necessitate parameter tweaking to match the assembly house set-up. The assembly house internal expertise usually evolves the suitable process.