

# **Dual P-Channel 20-V (D-S) MOSFET**

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	$R_{DS(on)}\left(\Omega\right)$	I <sub>D</sub> (A)		
- 20	$0.019 \text{ at V}_{GS} = -10 \text{ V}$	- 8.4		
	0.031 at V <sub>GS</sub> = - 4.5 V	- 6.7		

#### **FEATURES**

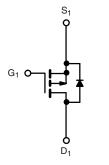
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>g</sub> Tested
- Compliant to RoHS Directive 2002/95/EC

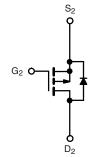


FREE

#### **APPLICATIONS**

- · Load Switching
  - Computer
  - Game Systems
- Battery Switching
  - 2-Cell Li-Ion





Ordering Information: Si4943BDY-T1-E3 (Lead (Pb)-free)

Top View

SO-8

 $S_2$ 

Si4943BDY-T1-GE3 (Lead (Pb)-free and Halogen-free)

D<sub>1</sub>

 $D_2$   $D_2$ 

P-Channel MOSFET

P-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATINGS</b>	T <sub>A</sub> = 25 °C, unles	ss otherwise n	oted		_
Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V <sub>DS</sub>	- 20		V
Gate-Source Voltage		$V_{GS}$	± 20		V
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 25 °C	1	- 8.4	- 6.3	^
	T <sub>A</sub> = 70 °C	- I <sub>D</sub>	- 6.7	- 5.1	
Pulsed Drain Current		I <sub>DM</sub>	- 30		Α
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	- 1.7	- 0.9	
	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2.0	1.1	14/
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 70 °C	L LD	1.3	0.7	W
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stq</sub>	- 55	to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
	t ≤ 10 s	R <sub>thJA</sub>	46	62.5	
Maximum Junction-to-Ambient <sup>a</sup>	Steady State	' 'thJA	85	110	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R <sub>thJF</sub>	26	35	

#### Notes:

a. Surface Mounted on 1" x 1" FR4 board.

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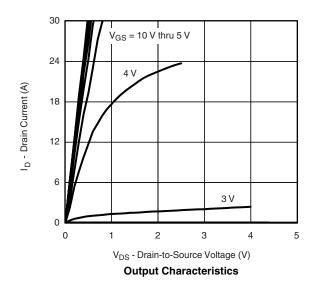
<b>SPECIFICATIONS</b> T <sub>J</sub> = 25 °C, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 1		- 3	V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zava Cata Valtaga Drain Current	1	$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}$			- 1	- 1 - 5 μΑ	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			- 5		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = - 5 V, V <sub>GS</sub> = - 10 V	- 30			Α	
	D	V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 8.4 A		0.016	0.019	0	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 6.7 A		0.026	0.031	Ω	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = - 10 V, I <sub>D</sub> = - 8.4 A		20		S	
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	I <sub>S</sub> = - 1.7 A, V <sub>GS</sub> = 0 V		- 0.75	- 1.2	V	
Dynamic <sup>b</sup>							
Total Gate Charge	$Q_g$			17	25		
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = -10 \text{ V}, V_{GS} = -5 \text{ V}, I_{D} = -8.4 \text{ A}$		5		nC	
Gate-Drain Charge	$Q_{gd}$			6.7			
Gate Resistance	$R_g$	f = 1 MHz	2.4	12	18	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			11	17		
Rise Time	t <sub>r</sub>	$V_{DD}$ = - 10 V, $R_L$ = 10 $\Omega$		10	15		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D\cong$ - 1 A, $V_{GEN}=$ - 10 V, $R_g=6~\Omega$		94	140	ns	
Fall Time	t <sub>f</sub>			60	90		
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = - 1.7 A, dl/dt = 100 A/μs		55	80		

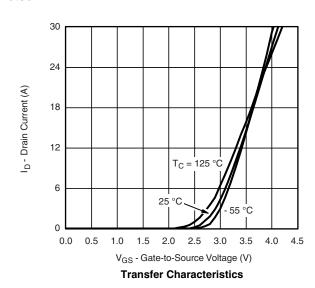
#### Notes:

- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



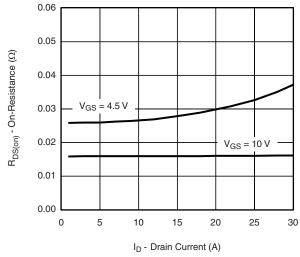




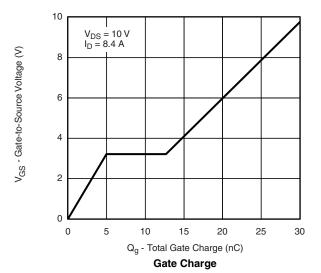


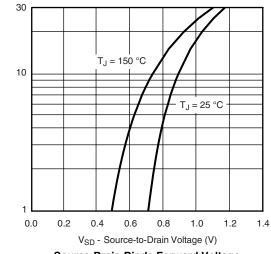


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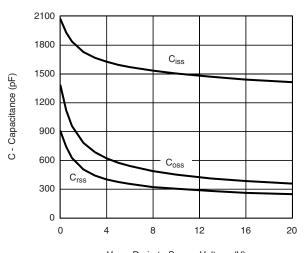


#### On-Resistance vs. Drain Current



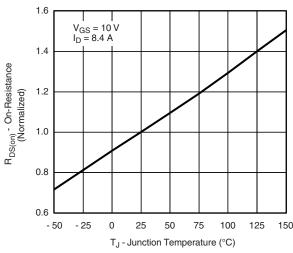


Source-Drain Diode Forward Voltage

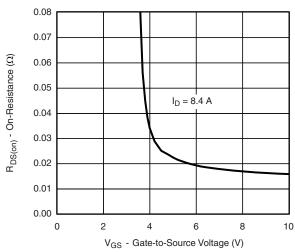


V<sub>DS</sub> - Drain-to-Source Voltage (V)





On-Resistance vs. Junction Temperature



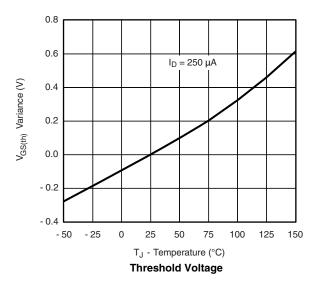
On-Resistance vs. Gate-to-Source Voltage

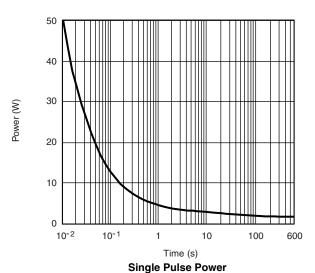
S - Source Current (A)

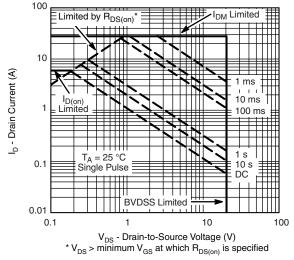
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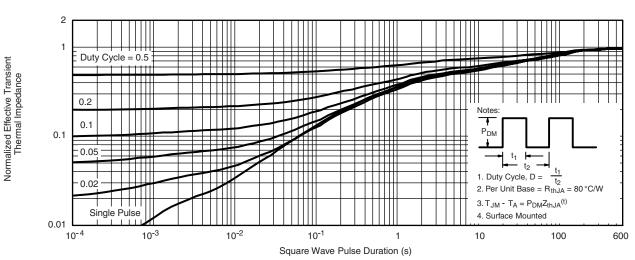
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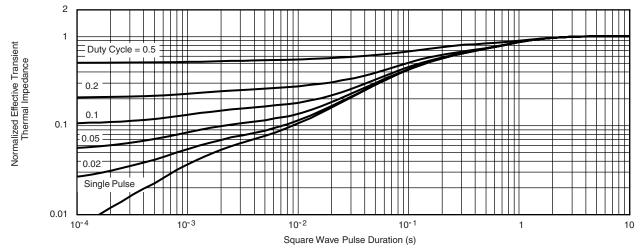
Safe Operating Area, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Ambient



## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Foot

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SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIM	IETERS	INCHES			
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A <sub>1</sub>	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
Е	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050 BSC			
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
FCN: C-06527-Bey   11-Sen-06						

DWG: 5498

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#### **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)

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