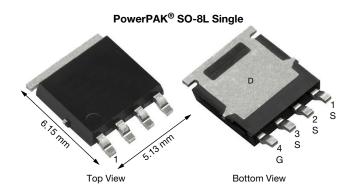


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Vishay Siliconix

# Automotive N-Channel 60 V (D-S) 175 °C MOSFET



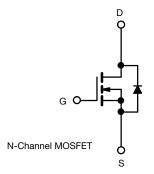
PRODUCT SUMMARY	
V <sub>DS</sub> (V)	60
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.0045
$R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 \text{ V}$	0.0062
I <sub>D</sub> (A)	75
Configuration	Single
Package	PowerPAK SO-8L

#### **FEATURES**

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R<sub>q</sub> and UIS tested
- Material categorization: for definitions of compliance please see www.vishav.com/doc?99912



ROHS COMPLIANT HALOGEN FREE



PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-source voltage	$V_{DS}$	60			
Gate-source voltage	$V_{GS}$	± 20	V		
Continuous drain current	T <sub>C</sub> = 25 °C <sup>a</sup>	1	75		
	T <sub>C</sub> = 125 °C	- I <sub>D</sub>	48		
Continuous source current (diode conduction	on) <sup>a</sup>	Is	60	Α	
Pulsed drain current <sup>b</sup>	I <sub>DM</sub>	140			
Single pulse avalanche current		I <sub>AS</sub>	42		
Single pulse avalanche energy	L = 0.1 mH	E <sub>AS</sub>	88	mJ	
Maximum power dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	P <sub>D</sub>	68	W	
	T <sub>C</sub> = 125 °C		22		
Operating junction and storage temperature	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C		
Soldering recommendations (peak temperature) d, e		-	260	-0	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount c	$R_{thJA}$	68	°C/W
Junction-to-case (drain)		$R_{thJC}$	2.2	C/VV

#### Notes

- a. Package limited
- b. Pulse test; pulse width  $\leq 300~\mu\text{s},$  duty cycle  $\leq 2~\%$
- c. When mounted on 1" square PCB (FR4 material)
- d. See solder profile (<a href="https://www.vishay.com/doc?73257">www.vishay.com/doc?73257</a>). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



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PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT		
Static								
Drain-source breakdown voltage	V <sub>DS</sub>	$V_{GS} = 0$ , $I_D = 250 \mu\text{A}$		60	-	-	V	
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$		1.5	2.0	2.5		
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	0 V, V <sub>GS</sub> = ± 20 V	-	-	± 100	nA	
	I <sub>DSS</sub>	$V_{GS} = 0 V$	V <sub>DS</sub> = 60 V	-	-	1		
Zero gate voltage drain current		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V, T <sub>J</sub> = 125 °C	-	-	50	μΑ	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V, T <sub>J</sub> = 175 °C	-	-	250		
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	$V_{DS} \ge 5 \text{ V}$	30	-	-	Α	
	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 10 A	-	0.0037	0.0045	Ω	
During and the second		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 8 A	-	0.0051	0.0062		
Drain-source on-state resistance <sup>a</sup>		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 10 A, T <sub>J</sub> = 125 °C	-	-	0.0071		
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 10 A, T <sub>J</sub> = 175 °C	-	-	0.0087		
Forward transconductance b	9fs	V <sub>DS</sub>	= 15 V, I <sub>D</sub> = 10 A	-	70	-	S	
Dynamic <sup>b</sup>								
Input capacitance	C <sub>iss</sub>		V <sub>DS</sub> = 25 V, f = 1 MHz	-	3900	5100	pF	
Output capacitance	Coss	$V_{GS} = 0 V$		-	1700	2300		
Reverse transfer capacitance	C <sub>rss</sub>			-	50	80		
Total gate charge <sup>c</sup>	Qg		V <sub>DS</sub> = 30 V, I <sub>D</sub> = 5 A	-	55	85	nC	
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V		-	12	-		
Gate-drain charge c	Q <sub>gd</sub>				8	-	1	
Gate resistance	$R_g$	f = 1 MHz		0.2	0.43	0.65	Ω	
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>	$V_{DD} = 30 \text{ V, } R_L = 6 \Omega$ $I_D \cong 5 \text{ A, } V_{GEN} = 10 \text{ V, } R_g = 1 \Omega$		-	17	35	- ns	
Rise time <sup>c</sup>	t <sub>r</sub>			-	5	10		
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>			-	32	50		
Fall time <sup>c</sup>	t <sub>f</sub>			-	14	25		
Source-Drain Diode Ratings and Charac	teristics b				•			
Pulsed current a	I <sub>SM</sub>			-	-	140	Α	
Forward voltage	V <sub>SD</sub>	I <sub>F</sub> = 10 A, V <sub>GS</sub> = 0		-	0.79	1.2	V	
Body diode reverse recovery time	t <sub>rr</sub>			-	62	130	ns	
Body diode reverse recovery charge	$Q_{rr}$	I <sub>F</sub> = 10 A, di/dt = 100 A/μs		-	107	220	nC	
Reverse recovery fall time	ta			-	31	-		
Reverse recovery rise time	t <sub>b</sub>			-	32	-	ns	
Body diode peak reverse recovery current	I <sub>RM(REC)</sub>			-	-3.1	-7	Α	

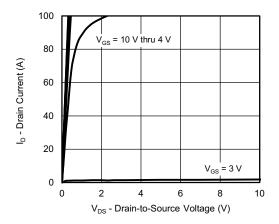
#### Notes

- a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

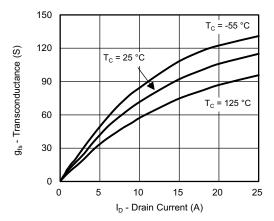
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



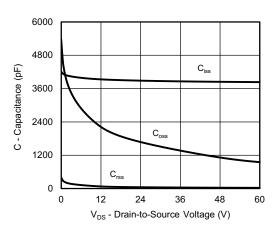
## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



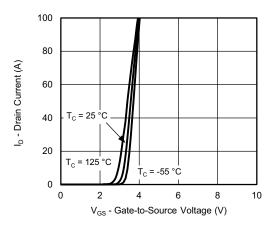
### **Output Characteristics**



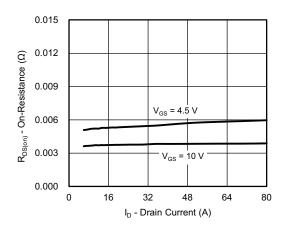
Transconductance



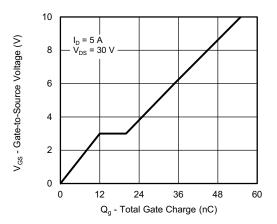
Capacitance



**Transfer Characteristics** 



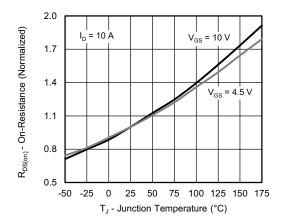
On-Resistance vs. Drain Current



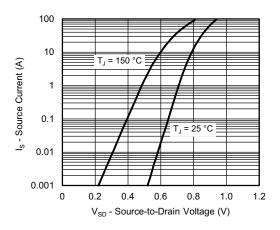
**Gate Charge** 



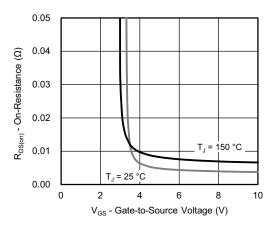
## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



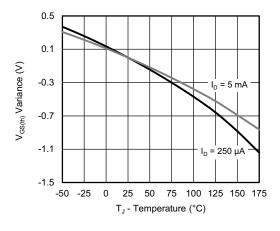
On-Resistance vs. Junction Temperature



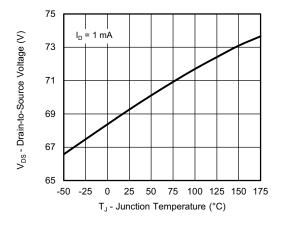
**Source Drain Diode Forward Voltage** 



On-Resistance vs. Gate-to-Source Voltage



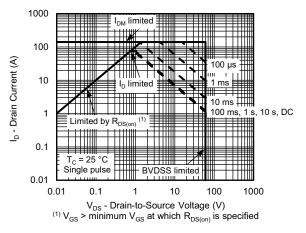
**Threshold Voltage** 



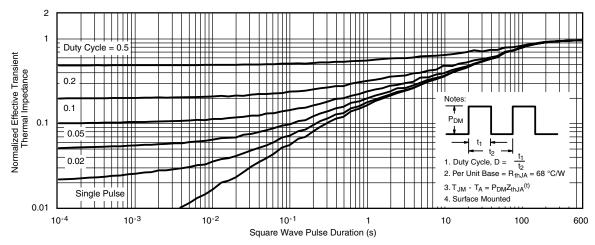
Drain Source Breakdown vs. Junction Temperature



## **THERMAL RATINGS** ( $T_A = 25$ °C, unless otherwise noted)



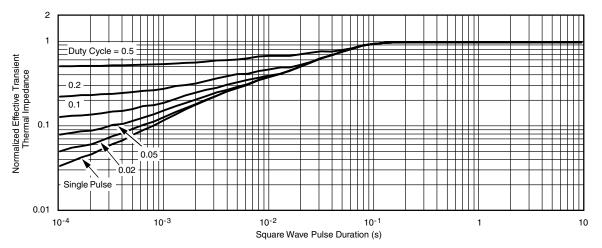
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



## THERMAL RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

#### Note

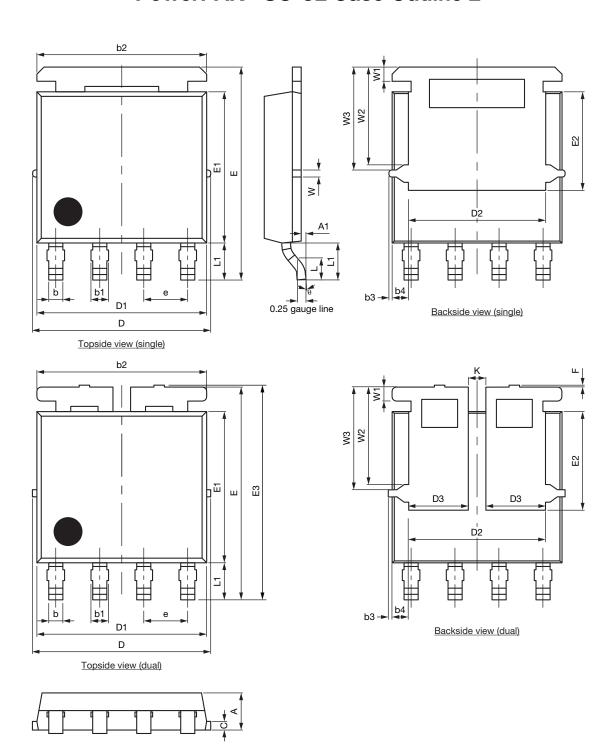
- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg275098">www.vishay.com/ppg275098</a>.



# PowerPAK® SO-8L Case Outline 2





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DIM		MILLIMETERS		INCHES				
DIM.	MIN.	NOM.	MAX.	MIN. NOM.		MAX.		
Α	1.00	1.07	1.14	0.039	0.042	0.045		
A1	0.00	-	0.127	0.00	-	0.005		
b	0.33	0.41	0.48	0.013	0.016	0.019		
b1	0.44	0.51	0.58	0.017	0.020	0.023		
b2	4.80	4.90	5.00	0.189	0.193	0.197		
b3		0.094			0.004			
b4		0.47			0.019			
С	0.20	0.25	0.30	0.008	0.010	0.012		
D	5.00	5.13	5.25	0.197	0.202	0.207		
D1	4.80	4.90	5.00	0.189	0.193	0.197		
D2	3.86	3.96	4.06	0.152	0.156	0.160		
D3	1.63	1.73	1.83	0.064	0.068	0.072		
е		1.27 BSC			0.050 BSC			
Е	6.05	6.15	6.25	0.238	0.242	0.246		
E1	4.27	4.37	4.47	0.168	0.172	0.176		
E2	2.75	2.85	2.95	0.108	0.112	0.116		
E3	6.05	6.22	6.40	0.238	0.245	0.252		
F	-	-	0.15	-	-	0.006		
L	0.62	0.72	0.82	0.024	0.028	0.032		
L1	0.92	1.07	1.22	0.036	0.042	0.048		
K	0.51			0.020				
W	0.23			0.009				
W1	0.41			0.016				
W2	2.82			0.111				
W3		2.96			0.117			
θ	0°	-	10°	0°	-	10°		

DWG: 6044

#### Note

• Millimeters will govern



### RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L SINGLE



Recommended Minimum Pads Dimensions in mm (inches)



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