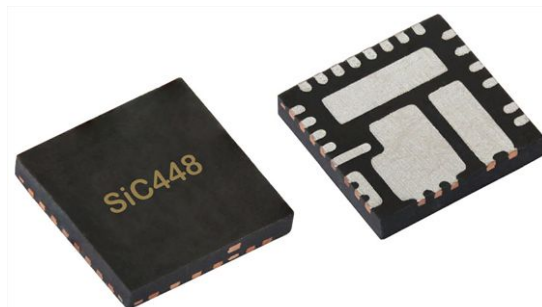


## 4.5 V to 45 V Input, 6 A, microBUCK® DC/DC Converter



### DESCRIPTION

The SiC448 is a wide input voltage, high efficiency synchronous buck regulator with integrated high side and low side power MOSFETs. Its power stage is capable of supplying high continuous current at a switching frequency up to 2 MHz. This regulator produces an adjustable output voltage down to 0.8 V from a 4.5 V to 45 V input rail to accommodate a variety of applications, including computing, consumer electronics, telecom, and industrial.

The SiC448's architecture allows for ultrafast transient response with minimum output capacitance and tight ripple regulation at very light load. The device enables loop stability regardless of the type of output capacitor used, including low ESR ceramic capacitors. The device also incorporates a power saving scheme that significantly increases light load efficiency. The regulator integrates a full protection feature set, including overcurrent protection (OCP), output overvoltage protection (OVP), short circuit protection (SCP), output undervoltage protection (UVP) and overtemperature protection (OTP). It also has UVLO for input rail and a user programmable soft start.

The SiC448 is available in a 6 A pin compatible 5 mm by 5 mm lead (Pb)-free power enhanced PowerPAK® MLP55-27L package.

### TYPICAL APPLICATION CIRCUIT

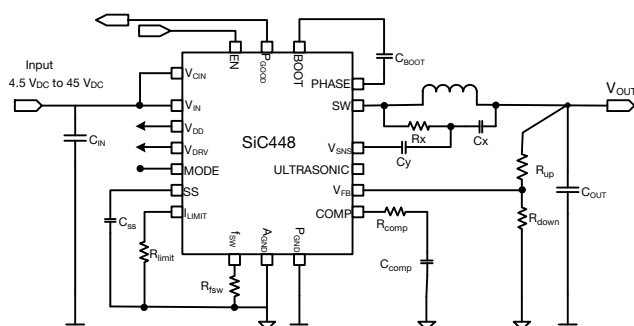


Fig. 1 - Typical Application Circuit

### FEATURES

- Versatile
  - Single supply operation from 4.5 V to 45 V input voltage
  - Adjustable output voltage down to 0.8 V
  - Scalable solution available: SiC46x / SiC47x series
  - Output voltage tracking and sequencing with pre-bias start up
  - $\pm 1\%$  output voltage accuracy at  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$
- Highly efficient
  - 98 % peak efficiency
  - 4  $\mu\text{A}$  supply current at shutdown
  - 235  $\mu\text{A}$  operating current, not switching
- Highly configurable
  - Adjustable switching frequency from 100 kHz to 2 MHz
  - Adjustable soft start and adjustable current limit
  - 3 modes of operation: forced continuous conduction, power save, or ultrasonic
- Robust and reliable
  - Output overvoltage and output overcurrent protection
  - Rugged 60 V Trench MOSFET UIS tested
- Design support tools
  - PowerCAD online design tool ([vishay.transim.com](http://vishay.transim.com)) for external component selection, SIMPLIS power supply system simulation, and efficiency and thermal simulations
- Material categorization: for definitions of compliance please see [www.vishay.com/doc/299912](http://www.vishay.com/doc/299912)



**RoHS**  
COMPLIANT  
HALOGEN  
FREE

### APPLICATIONS

- Industrial and automation
- Home automation
- Industrial and server computing
- Networking, telecom, and base station power supplies
- Unregulated wall transformers
- Robotics
- High end hobby electronics: remote control cars, planes, and drones
- Battery management systems
- Power tools
- Vending, ATM, and slot machines

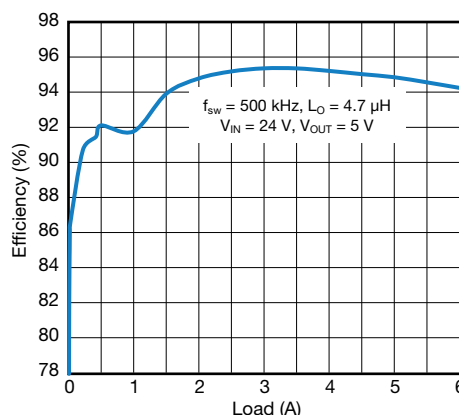


Fig. 2 - Efficiency vs. Output Current

## PIN CONFIGURATION

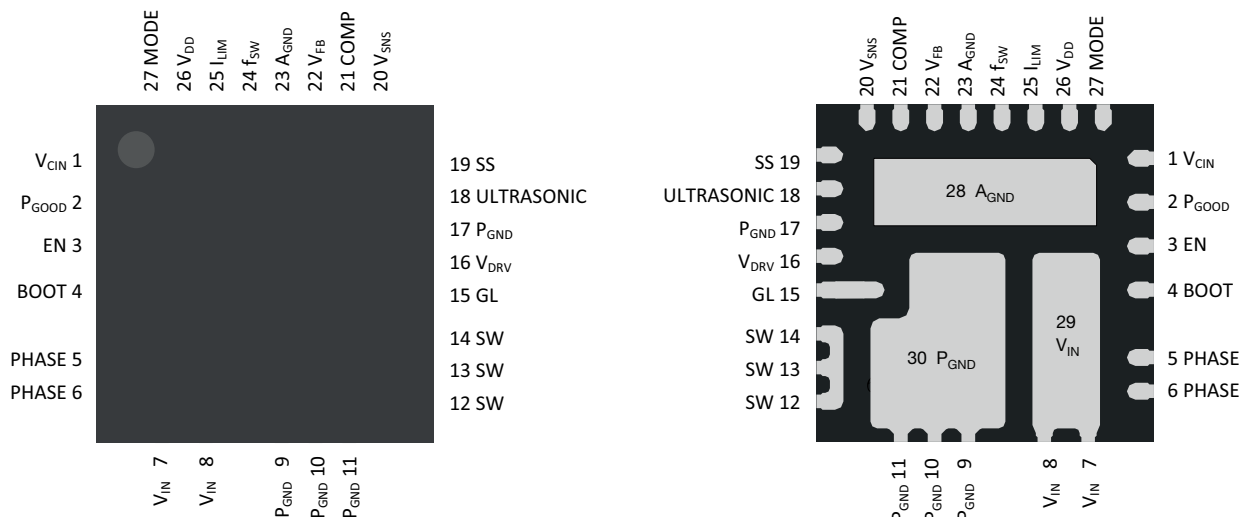
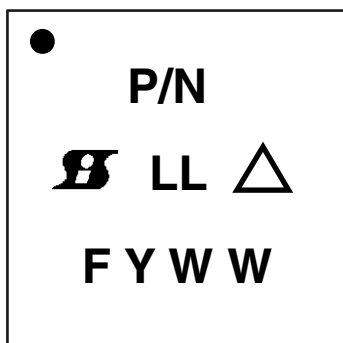


Fig. 3 - Pin Configuration

PIN DESCRIPTION		
PIN NUMBER	SYMBOL	DESCRIPTION
1	$V_{CIN}$	Supply voltage for internal regulators $V_{DD}$ and $V_{DRV}$ . This pin should be tied to $V_{IN}$ , but can also be connected to a lower supply voltage ( $> 5\text{ V}$ ) to reduce losses in the internal linear regulators
2	$P_{GOOD}$	Open-drain power good indicator - high impedance indicates power is good. An external pull-up resistor is required
3	EN	Enable pin. Tie high/low to enable / disable the IC accordingly. This is a high voltage compatible pin, can be tied to 45 V
4	BOOT	High side driver bootstrap voltage
5, 6	PHASE	Return path of high side gate driver
7, 8, 29	$V_{IN}$	Power stage input voltage. Drain of high side MOSFET
9, 10, 11, 17, 30	$P_{GND}$	Power ground
12, 13, 14	SW	Power stage switch node
15	GL	Low side MOSFET gate signal
16	$V_{DRV}$	Supply voltage for internal gate driver. When using the internal LDO as a bias power supply, $V_{DRV}$ is the LDO output. Connect a 4.7 $\mu\text{F}$ decoupling capacitor to $P_{GND}$
18	ULTRASONIC	Float to disable ultrasonic mode, connect to $V_{DD}$ to enable. Depending on the operation mode set by the mode pin, power save mode or forced continuous mode will be enabled when the ultrasonic mode is disabled
19	SS	Set the soft start ramp by connecting a capacitor to $A_{GND}$ . An internal current source will charge the capacitor
20	$V_{SNS}$	Power inductor signal feedback pin for system stability compensation
21	COMP	Output of the internal error amplifier. The feedback loop compensation network is connected from this pin to the $A_{GND}$ pin
22	$V_{FB}$	Feedback input for switching regulator used to program the output voltage - connect to an external resistor divider from $V_{OUT}$ to $A_{GND}$
23, 28	$A_{GND}$	Analog ground
24	$f_{SW}$	Set the on-time by connecting a resistor to $A_{GND}$
25	$I_{LIMIT}$	Set the current limit by connecting a resistor to $A_{GND}$
26	$V_{DD}$	Bias supply for the IC. $V_{DD}$ is an LDO output, connect a 1 $\mu\text{F}$ decoupling capacitor to $A_{GND}$
27	MODE	Set various operation modes by connecting a resistor to $A_{GND}$ . See specification table for details

ORDERING INFORMATION		
PART NUMBER	PACKAGE	MARKING CODE
SiC448ED-T1-GE3	PowerPAK <sup>®</sup> MLP55-27L	SiC448
SiC448EVB	Reference board	

**PART MARKING INFORMATION**


- = pin 1 indicator
- P/N = part number code
- B** = Siliconix logo
- △ = ESD symbol
- F = assembly factory code
- Y = year code
- WW = week code
- LL = lot code

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)			
ELECTRICAL PARAMETER	CONDITIONS	LIMITS	UNIT
V <sub>CIN</sub> , V <sub>IN</sub>	Reference to P <sub>GND</sub>	-0.3 to 50	V
EN	Reference to A <sub>GND</sub>	-0.3 to 50	
SW / PHASE	Reference to P <sub>GND</sub>	-0.3 to 50	
V <sub>DRV</sub>	Reference to P <sub>GND</sub>	-0.3 to 6	
V <sub>DD</sub>	Reference to A <sub>GND</sub>	-0.3 to 6	
SW / PHASE (AC)	Reference to P <sub>GND</sub> ; 100 ns	-0.3 to 50	
BOOT		-0.3 to V <sub>PHASE</sub> + V <sub>DRV</sub>	
A <sub>GND</sub> to P <sub>GND</sub>		-0.3 to 0.3	
All other pins	Reference to A <sub>GND</sub>	-0.3 to V <sub>DD</sub> + 0.3	
Temperature			
Junction temperature	T <sub>J</sub>	-40 to +150	°C
Storage temperature	T <sub>STG</sub>	-65 to +150	
Power Dissipation			
Thermal resistance from junction-to-ambient		12	°C/W
Thermal resistance from junction-to-case		2	
ESD Protection			
Electrostatic discharge protection	Human body model, JESD22-A114	2000	V
	Charged device model, JESD22-A101	500	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (all voltages referenced to GND = 0 V)				
PARAMETER	MIN.	TYP.	MAX.	UNIT
Input voltage (V <sub>IN</sub> )	4.5	-	45	V
Control input voltage (V <sub>CIN</sub> ) <sup>(1)</sup>	4.5	-	45	
Enable (EN)	0	-	45	
Bias supply (V <sub>DD</sub> )	4.75	5	5.25	
Drive supply voltage (V <sub>DRV</sub> )	4.75	5.3	5.55	
Output voltage (V <sub>OUT</sub> )	0.8	-	0.92 x V <sub>IN</sub>	
Temperature				
Recommended ambient temperature	-40 to +105			°C
Operating junction temperature	-40 to +125			

**Note**

(1) For input voltages below 5 V, provide a separate supply to  $V_{CIN}$  of at least 5 V to prevent the internal  $V_{DD}$  rail UVLO from triggering



ELECTRICAL SPECIFICATIONS (V <sub>IN</sub> = V <sub>CIN</sub> = 24 V, V <sub>EN</sub> = 5 V, T <sub>J</sub> = -40 °C to +125 °C, unless otherwise stated)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power Supplies						
V <sub>DD</sub> supply	V <sub>DD</sub>	V <sub>IN</sub> = V <sub>CIN</sub> = 6 V to 45 V	4.75	5	5.25	V
		V <sub>IN</sub> = V <sub>CIN</sub> = 5 V	4.7	5	-	
V <sub>DD</sub> dropout	V <sub>DD_DROPOUT</sub>	V <sub>IN</sub> = V <sub>CIN</sub> = 5 V, I <sub>VDD</sub> = 1 mA	-	120	-	mV
V <sub>DD</sub> UVLO threshold, rising	V <sub>DD_UVLO</sub>		4	4.25	4.5	V
V <sub>DD</sub> UVLO hysteresis	V <sub>DD_UVLO_HYST</sub>		-	225	-	mV
Maximum V <sub>DD</sub> current	I <sub>DD</sub>	V <sub>IN</sub> = V <sub>CIN</sub> = 6 V to 45 V	3	-	-	mA
V <sub>DRV</sub> supply	V <sub>DRV</sub>	V <sub>IN</sub> = V <sub>CIN</sub> = 6 V to 45 V	5.1	5.4	5.65	V
		V <sub>IN</sub> = V <sub>CIN</sub> = 5 V	4.8	5	5.2	
V <sub>DRV</sub> dropout	V <sub>DRV_DROPOUT</sub>	V <sub>IN</sub> = V <sub>CIN</sub> = 5 V, I <sub>VDD</sub> = 10 mA	-	240	-	mV
Maximum V <sub>DRV</sub> current	V <sub>DRV</sub>	V <sub>IN</sub> = V <sub>CIN</sub> = 6 V to 45 V	50	-	-	mA
V <sub>DRV</sub> UVLO threshold, rising	V <sub>DRV_UVLO</sub>		4	4.25	4.5	V
V <sub>DRV</sub> UVLO hysteresis	V <sub>DRV_UVLO_HYST</sub>		-	295	-	mV
Input current	I <sub>VCIN</sub>	Non-switching, V <sub>FB</sub> > 0.8 V	-	235	325	μA
Shutdown current	I <sub>VCIN_SHDN</sub>	V <sub>EN</sub> = 0 V	-	4	8	
Controller and Timing						
Feedback voltage	V <sub>FB</sub>	T <sub>J</sub> = 25 °C	796	800	804	mV
		T <sub>J</sub> = -40 °C to +125 °C <sup>(1)</sup>	792	800	808	
V <sub>FB</sub> input bias current	I <sub>FB</sub>		-	2	-	nA
Transconductance	g <sub>m</sub>		-	0.3	-	mS
COMP source current	I <sub>COMP_SOURCE</sub>		15	20	-	μA
COMP sink current	I <sub>COMP_SINK</sub>		15	20	-	
Minimum on-time	t <sub>ON_MIN.</sub>		-	90	110	ns
t <sub>ON</sub> accuracy	t <sub>ON_ACCURACY</sub>		-10	-	10	%
On-time range	t <sub>ON_RANGE</sub>		110	-	8000	ns
Frequency range	f <sub>sw</sub>	Ultrasonic mode enabled	20	-	2000	kHz
		Ultrasonic mode disabled	0	-	2000	
Minimum off-time	t <sub>OFF_MIN.</sub>		190	250	310	ns
Soft start current	I <sub>SS</sub>		3	5	7	μA
Soft start voltage	V <sub>SS</sub>	When V <sub>OUT</sub> reaches regulation	-	1.5	-	V
Fault Protections						
Valley current limit	I <sub>OCP</sub>	R <sub>ILIM</sub> = 60 kΩ, T <sub>J</sub> = -10 °C to +125 °C <sup>(2)</sup>	5.6	7.0	8.4	A
Output OVP threshold	V <sub>OVP</sub>	V <sub>FB</sub> with respect to 0.8 V reference	-	20	-	%
Output UVP threshold	V <sub>UVP</sub>		-	-80	-	
Overtemperature protection	T <sub>OTP_RISING</sub>	Rising temperature	-	150	-	°C
	T <sub>OTP_HYST</sub>	Hysteresis	-	35	-	
Power Good						
Power good output threshold	V <sub>FB_RISING_VTH_OV</sub>	V <sub>FB</sub> rising above 0.8 V reference	-	20	-	%
	V <sub>FB_FALLING_VTH_UV</sub>	V <sub>FB</sub> falling below 0.8 V reference	-	-10	-	
Power good hysteresis	V <sub>FB_HYST</sub>		-	50	-	mV
Power good on resistance	R <sub>ON_PGOOD</sub>		-	7.5	15	Ω
Power good delay time	t <sub>DLY_PGOOD</sub>		15	25	35	μs

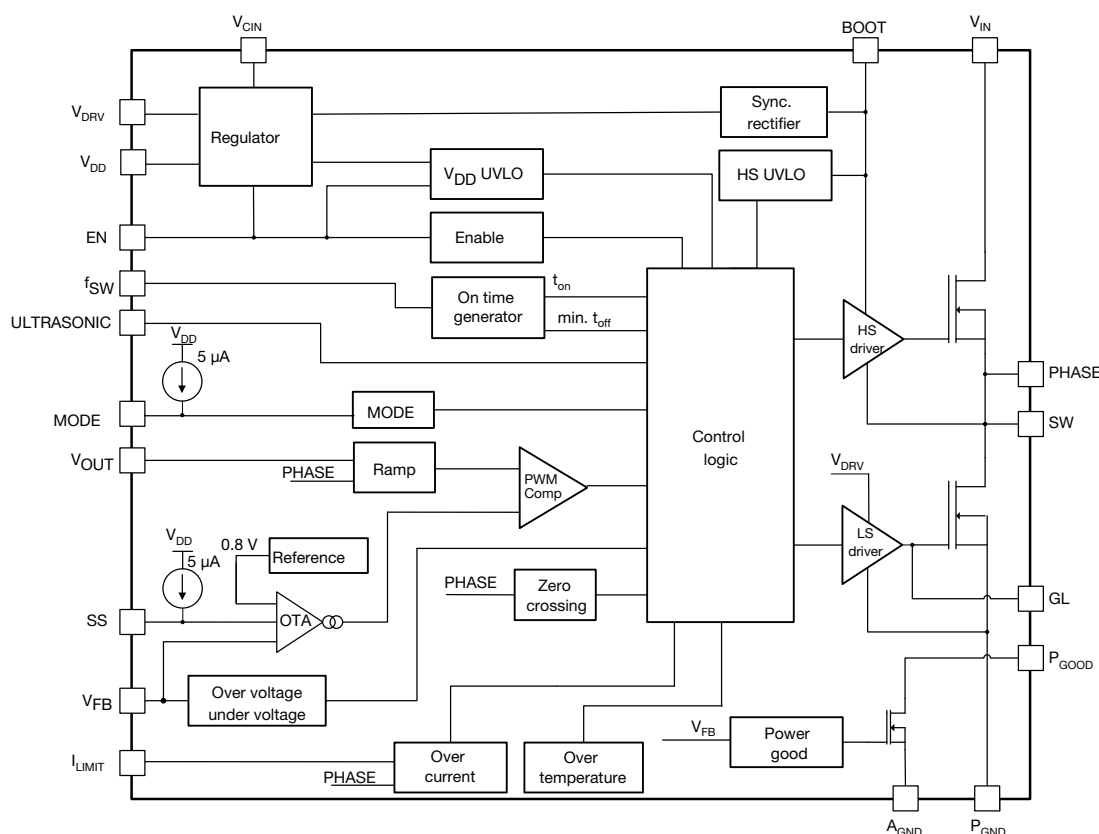


<b>ELECTRICAL SPECIFICATIONS</b> ( $V_{IN} = V_{CIN} = 24\text{ V}$ , $V_{EN} = 5\text{ V}$ , $T_J = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ , unless otherwise stated)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>EN / MODE / Ultrasonic Threshold</b>						
EN logic high level	$V_{EN\_H}$		-	1.35	-	V
EN logic low level	$V_{EN\_L}$		-	1.2	-	
EN hysteresis	$V_{HYST}$		-	0.15	-	
EN pull down resistance	$R_{EN}$		-	5	-	M $\Omega$
Ultrasonic mode high Level	$V_{ULTRASONIC\_H}$		2	-	-	V
Ultrasonic mode low level	$V_{ULTRASONIC\_L}$		-	-	0.8	
Mode pull up current	$I_{MODE}$		3.75	5	6.25	$\mu\text{A}$
Mode 1	$R_{MODE}$	Power save mode enabled, $V_{DD}$ , $V_{DRV}$ Pre-reg on	0	2	100	k $\Omega$
Mode 2		Power save mode disabled, $V_{DD}$ , $V_{DRV}$ Pre-reg on	298	301	304	
Mode 3		Power save mode disabled, $V_{DRV}$ Pre-reg off, $V_{DD}$ Pre-reg on, provide external $V_{DRV}$	494	499	504	
Mode 4		Power save mode enabled, $V_{DRV}$ Pre-reg off, $V_{DD}$ Pre-reg on, provide external $V_{DRV}$	900	1000	1100	

**Notes**

- (1) Guaranteed by design  
 (2) Guaranteed by design for SiC448 OCP measurements

## FUNCTIONAL BLOCK DIAGRAM



**Fig. 4 - Functional Block Diagram**

## OPERATIONAL DESCRIPTION

### Device Overview

The SiC448 is a high efficiency synchronous buck regulator capable of delivering up to 6 A continuous current. The device has programmable switching frequency of 100 kHz to 2 MHz. The voltage mode, constant on time control scheme delivers fast transient response, minimizes the number of external components and enables loop stability regardless of the type of output capacitor used, including low ESR ceramic capacitors. The device also incorporates a power saving feature that enables diode emulation mode and frequency fold back as the load decreases.

The SiC448 has a full set of protection and monitoring features:

- Overcurrent protection in pulse-by-pulse mode
- Output overvoltage protection
- Output undervoltage protection with auto retry
- Overtemperature protection with hysteresis
- Dedicated enable pin for easy power sequencing
- Power good open drain output
- This device is available in the 5 mm by 5 mm lead (Pb)-free power enhanced PowerPAK. MLP55-27L package to deliver high power density and minimize PCB area

### Power Stage

The SiC448 integrates a high performance power stage with a n-channel high side MOSFET and a n-channel low side MOSFET optimized to achieve up to 98 % efficiency.

The power input voltage ( $V_{IN}$ ) can go up to 45 V and down as low as 4.5 V for power conversion.

### Control Scheme

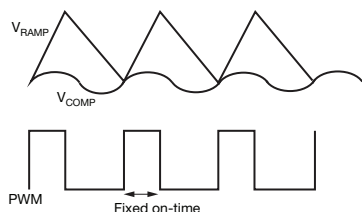
The SiC448 employs a voltage mode COT control mechanism in conjunction with adaptive zero current detection which allows for power saving in discontinuous conduction mode (DCM). The switching frequency,  $f_{SW}$ , is set by an external resistor to  $A_{GND}$ ,  $R_{fsw}$ . The SiC448 operates between 100 kHz to 2 MHz depending on  $V_{IN}$  and  $V_{OUT}$  conditions.

$$R_{fsw} = \frac{V_{OUT}}{f_{SW} \times 190 \times 10^{-12}}$$

Note, as long as  $V_{IN}$  and  $V_{CIN}$  are connected together,  $f_{SW}$  has no dependency on  $V_{IN}$  as the on time is adjusted as  $V_{IN}$  varies. During steady-state operation, feedback voltage ( $V_{FB}$ ) is compared with internal reference (0.8 V typ.) and the amplified error signal ( $V_{COMP}$ ) is generated at the comp node by the external compensation components,  $R_{COMP}$  and  $C_{COMP}$ . An externally generated ramp signal and  $V_{COMP}$  feed into a comparator. Once  $V_{RAMP}$  crosses  $V_{COMP}$ , an on-time pulse is generated for a fixed time. During the on-time pulse, the high side MOSFET will be turned on. Once the on-time

pulse expires, the low side MOSFET will be turned on after a dead time period. The low side MOSFET will stay on for a minimum duration equal to the minimum off-time ( $t_{OFF\_MIN.}$ ) and remains on until  $V_{RAMP}$  crosses  $V_{COMP}$ . The cycle is then repeated.

Fig. 6 illustrates the basic block diagram for voltage mode, constant on time architecture with external ripple injection,  $V_{RAMP}$ , while Fig. 5 illustrates the basic operational principle.



**Fig. 5 - Operational Principle**

The need for ripple injection in this architecture is explained below. First, let us understand the basic principles of this control architecture:

- The reference of a basic voltage mode COT regulator is replaced with a high gain error amplifier loop. The loop ensures the DC component of the output voltage follows the internal accurate reference voltage, providing excellent regulation
- A second voltage feedback path via  $V_{SNS}$  with a  $V_{RAMP}$  scheme ensures rapid correction of the transient perturbation
- This establishes two voltage loops, one is the steady state voltage feedback path (via the FB pin) and the other is the feed forward path (via the  $V_{SNS}$  pin). The scheme gives the user the fast transient response of a COT regulator and the stable, jitter free, line and load regulation performance of a PWM controller

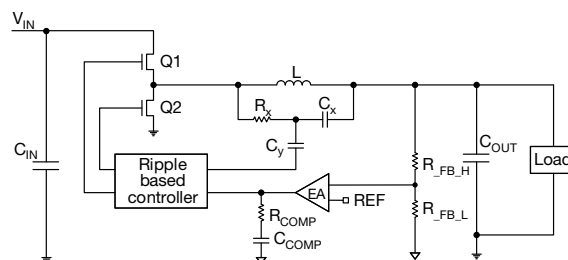
### Choosing the Ripple Injection Component Values

For stability purposes the SiC448 requires adequate ripple injection amplitude. Adequate ripple amplitude is required for two main reasons:

1. To reduce jitter due to noise coupled into the system
2. To provide stable operation. Sub harmonic oscillation can occur with constant on time ripple control if below condition is not met

$$ESR \times C_{OUT} > \frac{t_{ON}}{2}$$

Therefore, when the converter design uses an all ceramic output capacitor or other low ESR output capacitors, instability can occur. In order to avoid this, a  $V_{RAMP}$  network is used to increase the equivalent  $R_{ESR}$  in order to satisfy the above condition. The  $V_{RAMP}$  amplitude must be large enough to avoid instability or noise sensitivity but not too large that it degrades transient performance. To ensure stable operation under CCM, DCM and ultrasonic mode, minimum  $V_{RAMP}$  amplitude of 100 mV is recommended for the SiC448 family of regulators. A maximum  $V_{RAMP}$  of 900 mV is recommended so as not to degrade transient response.



**Fig. 6 - Control Block Diagram**

Below is the equation for calculating the  $V_{RAMP}$  amplitude.

$$V_{RAMP} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{(V_{IN} \times f_{sw} \times C_X \times R_X)}$$

$V_{RAMP}$  amplitude is a function of  $V_{IN}$ ,  $V_{OUT}$ , and switching frequency and should be adjusted whenever  $V_{IN}$ ,  $V_{OUT}$ , or switching frequency is changed.

For a given buck regulator design,  $V_{OUT}$  and switching frequency are typically fixed, while the converter may be expected to work for a wide  $V_{IN}$  range. The  $V_{RAMP}$  amplitude will increase as  $V_{IN}$  is increased and increase the power dissipated by  $R_X$ . A proper selection of  $R_X$ , package size, and value should take into account the maximum power dissipation at the expected operating conditions.

In order to optimize the  $V_{RAMP}$  amplitude over a desired  $V_{IN}$  range use the following procedure to calculate  $R_X$ ,  $C_X$ , and  $C_Y$ :

1. The equation below calculates  $R_X$  as a function of  $V_{IN}$ ,  $V_{OUT}$ , and maximum allowable power dissipated by  $R_X$ .

$$R_X = \frac{V_{IN\_MAX.} \times V_{OUT} \times (1 - D)}{P_{RX\_MAX.}}$$

where  $P_{RX\_MAX.}$  is the maximum allowed power dissipation in  $R_X$ . Note, the maximum power dissipation of a 0603 sized resistor is typically 25 mW. Power dissipation derating must be taken into account for high ambient temperatures

2. The equation below calculates  $C_{X\_MIN.}$  as a function of  $V_{IN}$  and maximum allowed  $V_{RAMP}$  amplitude.

$$C_{X\_MIN.} = \frac{P_{RX\_MAX.}}{V_{IN\_MAX.} \times f_{sw} \times V_{RAMP\_MAX.}}$$

where  $V_{RAMP\_MAX.} = 900$  mV

3. Using  $V_{RAMP}$  equation, calculate  $V_{RAMP\_MIN.}$  at minimum  $V_{IN}$  based on the  $R_X$  and the minimum  $C_X$  value calculated above
4. If  $V_{RAMP\_MIN.}$  is  $> 200$  mV, set  $C_X$  to  $C_{X\_MIN.}$ , otherwise set  $C_X$  to  $(C_{X\_MIN.} \times V_{RAMP\_MIN.}/200$  mV). If  $V_{RIPPLE\_MIN.}$  is  $< 100$  mV, increase  $P_{RX\_MAX.}$  and recalculate  $R_X$  and  $C_X$
5.  $C_Y$  should be large enough not to distort the  $V_{RAMP}$  and small enough not to load excessively the  $V_{RAMP}$  network ( $R_X$  and  $C_X$ ). Please use the follow formula:  $C_Y = 1/(820 \times f_{sw})$

This procedure allows for a maximum range of operation. In order to simplify the procedure for calculating  $V_{RAMP}$  and compensation components, a calculator is provided



(visit [www.vishay.com/doc?65124](http://www.vishay.com/doc?65124)).

### Error Amplifier Compensation Value Selection (for reference only)

$R_{COMP}$  and  $C_{COMP}$  in the Fig. 6 are the components used to compensate the control loop.

For optimal transient response, the crossover frequency should be:

- Set typically at 1/10<sup>th</sup> to 1/5<sup>th</sup> of the converter switching frequency (Vishay's component calculator tool uses 1/10<sup>th</sup> the converter switching frequency)
- Be above the LC filter resonance frequency which is  $1/2 \pi \sqrt{LC}$

The procedure to select the  $R_{COMP}$  and  $C_{COMP}$  such that the above conditions are met is as follows:

6. Plot the magnitude and phase of the control to output transfer function using the equation below.  
Control to output transfer function.

$$H(s) = A \times \frac{(1 + sR_C C_o) \times (1 + sR_x C_x) \times (1 + sR_y C_y)}{\left(1 + \frac{sL}{R_o} + s^2 LC_o\right) \times (1 + sR_x C_x) \times (1 + sR_y C_y) + AR_y C_y s \times \left[1 + s \times \left(R_x C_x + \frac{L}{R_o}\right) + s^2 \times (R_x R_C C_x C_o + LC_o)\right]}$$

Where  $A = (2V_{IN} \times R_x \times C_x \times f)/V_{OUT}$ ,  $R_x$ ,  $C_x$ ,  $C_y$  are components for ripple injection as shown in Fig. 6 and  $R_y$  is the internal impedance of the  $V_{SNS}$  pin and is = 65 k $\Omega$ .

$C_o$  - output capacitance

$R_C$  - output capacitor ESR

7. From the plot of the control to output transfer function, determine the gain and phase at the crossover frequency
8. Calculate the  $R_{COMP}$  using the equation

$$R_{COMP} = \frac{1}{G_H \times g_m \times r_{FB}}$$

where  $G_H$  is the gain of the transfer function at crossover frequency, " $g_m$ " is the transconductance of the error amplifier (300  $\mu$ S) and  $r_{FB}$  is the ratio of the feedback divider,  $r_{FB} = R_{FB\_L}/(R_{FB\_L} + R_{FB\_H})$

9. Select  $C_{COMP}$  based on the placement of the zero such that phase margin is sufficient at the crossover frequency. A phase margin of over 60° is sufficient for converter stability. A good starting point is to place the compensation zero at 1/5<sup>th</sup> of the LC pole

$$C_{COMP} = \frac{5\sqrt{LC}}{R_{COMP}}$$

Once the component values are calculated, it is now possible to calculate the total loop gain. The total loop gain is the product of the control to output transfer function and the error amplifier transfer function.

The transfer function of the error amplifier is given by the equation below.

$$G(s) = g_m R_o \times \frac{(1 + sR_{COMP} C_{COMP}) \times r_{FB}}{(1 + s \times (R_{COMP} C_{COMP} + R_o C_{COMP}))}$$

Where  $R_o = 40$  M $\Omega$  is the output resistance of the transconductance amplifier.

Total loop transfer function =  $H(s)G(s)$

An automated calculator (visit [www.vishay.com/doc?75760](http://www.vishay.com/doc?75760)) is provided to assist the user to determine  $V_{RAMP}$  components as well as error amplifier compensation components using user selected operating conditions.



## Power-Save Mode, Mode Pin, and Ultrasonic Pin Operation

To improve efficiency at light-loads, the SiC448 provides a set of innovative implementations to reduce low side re-circulating current and switching losses. The internal zero crossing detector monitors SW node voltage to determine when inductor current starts to flow negatively. In power saving mode, as soon as inductor current crosses zero, the device first deploys diode mode by turning off the low side MOSFET. If load further decreases, switching frequency is reduced proportional to the load condition to save switching losses while keeping output ripple within tolerance. If the ultrasonic pin is tied to  $V_{DD}$ , the minimum switching frequency in discontinuous mode is  $> 20$  kHz to avoid switching frequencies in the audible range. If this feature is not required ultrasonic mode can be disabled by floating the ULTRASONIC pin. When ultrasonic mode is disabled, the regulator will operate in forced continuous mode or power save mode where there is no limit to the lower frequency limit. In this state, at zero load, switching frequency can go as low as hundreds of hertz.

To improve the converter efficiency, the user can choose to

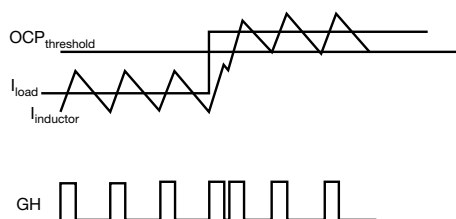
## OUTPUT MONITORING AND PROTECTION FEATURES

### Output Overcurrent Protection (OCP)

SiC448 has pulse-by-pulse overcurrent limit control. The inductor current is monitored during low side MOSFET conduction time through  $R_{DS(on)}$  sensing. After a pre-defined blanking time, the inductor current is compared with an internal OCP threshold. If inductor current is higher than OCP threshold, high side MOSFET is kept off until the inductor current falls below OCP threshold.

OCP is enabled immediately after  $V_{DD}$  passes UVLO level.

OCP is set by an external resistor,  $R_{LIM}$  to  $A_{GND}$ . (See table 2)



**Fig. 7 - Overcurrent Protection Illustration**

### Output Undervoltage Protection (UVP)

UVP is implemented by monitoring the FB pin. If the voltage level at FB drops below 0.16 V for more than 25  $\mu$ s, a UVP event is recognized and both high side and low side MOSFETs are turned off. After a duration equivalent to 20 soft start periods, the IC attempts to re-start. If the fault condition still exists, the above cycle will be repeated.

UVP is only active after the completion of soft-start sequence.

### Output Overvoltage Protection (OVP)

OVP is implemented by monitoring the FB pin. If the voltage level at FB rising above 0.96 V, an OVP event is recognized and both high side and low side MOSFETs are turned off. Normal operation is resumed once FB voltage drop below 0.91 V.

disable the internal  $V_{DRV}$  regulator by picking either mode 3 or mode 4 and connecting a 5 V supply to the  $V_{DRV}$  pin. This reduces power dissipation in the SiC448 by eliminating the  $V_{DRV}$  linear regulator losses.

The mode pin supports several modes of operation as shown in table 1. An internal current source is used to set the voltage on this pin using an external resistor:

**TABLE 1 - OPERATION MODES**

MODE	RANGE (k $\Omega$ )	POWER SAVE MODE	INTERNAL $V_{DRV}$ REGULATOR
1	0 to 100	Enabled	ON
2	298 to 304	Disabled	ON
3	494 to 504	Disabled	OFF <sup>(1)</sup>
4	900 to 1100	Enabled	OFF <sup>(1)</sup>

#### Note

<sup>(3)</sup> Connect a 5 V ( $\pm 5$  %) supply to the  $V_{DRV}$  pin

The mode pin is not latched to any state and can be changed on the fly.

### Overtemperature Protection (OTP)

OTP is implemented by monitoring the junction temperature. If the junction temperature rises above 150  $^{\circ}$ C, an OTP event is recognized and both high side and low MOSFETs are turned off. After the junction temperature falls below 115  $^{\circ}$ C (35  $^{\circ}$ C hysteresis), the device restarts by initiating a soft start sequence.

### Sequencing of Input / Output Supplies

The SiC448 has no sequencing requirements on its supplies or enables ( $V_{IN}$ ,  $V_{CIN}$ ,  $V_{DD}$ ,  $V_{DRV}$ , EN).

### Enable

The SiC448 has an enable pin to turn the part on and off. Driving this pin above 1.35 V enables the device, while driving the pin below 1.2 V disables the device.

The EN pin is internally pulled to  $A_{GND}$  by a 5 M $\Omega$  resistor to prevent unwanted turn on due to a floating GPIO.

### Soft-Start

During soft start time period, inrush current is limited and the output voltage is ramped gradually. The following control scheme is implemented:

Once the  $V_{DD}$  voltage reaches the UVLO trip point, an internal "Soft start Reference" (SR) begins to ramp up. The SR ramp rate is determined by the external soft start capacitor and an internal 5  $\mu$ A current source tied to the soft start pin.

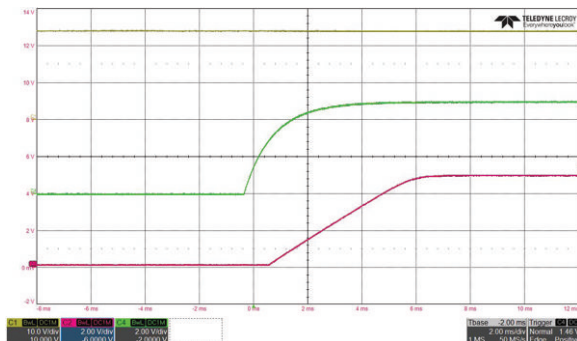
The internal SR signal is used as a reference voltage to the error amplifier (see functional block diagram). The control scheme guarantees that the output voltage during the soft start interval will ramp up coincidentally with the SR voltage. The soft-start time,  $t_{ss}$ , is adjustable by calculating a capacitor value from the following equation.

$$t_{ss} = \frac{C_{ss} \times 0.8 \text{ V}}{5 \mu\text{A}}$$

During soft-start period, OCP is activated. Short circuit protection is not active until soft-start is complete.

## Pre-Bias Start-Up

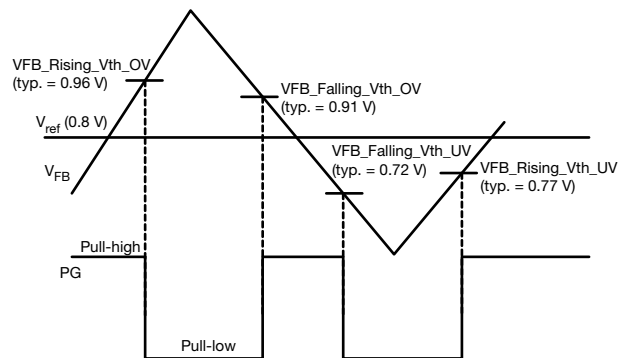
In case of pre-bias startup, output is monitored through FB pin. If the sensed voltage on FB is higher than the internal reference ramp value, control logic prevents high side and low side MOSFETs from switching to avoid negative output voltage spike and excessive current sinking through low side MOSFET.



**Fig. 8 - Pre-Bias Start-Up**

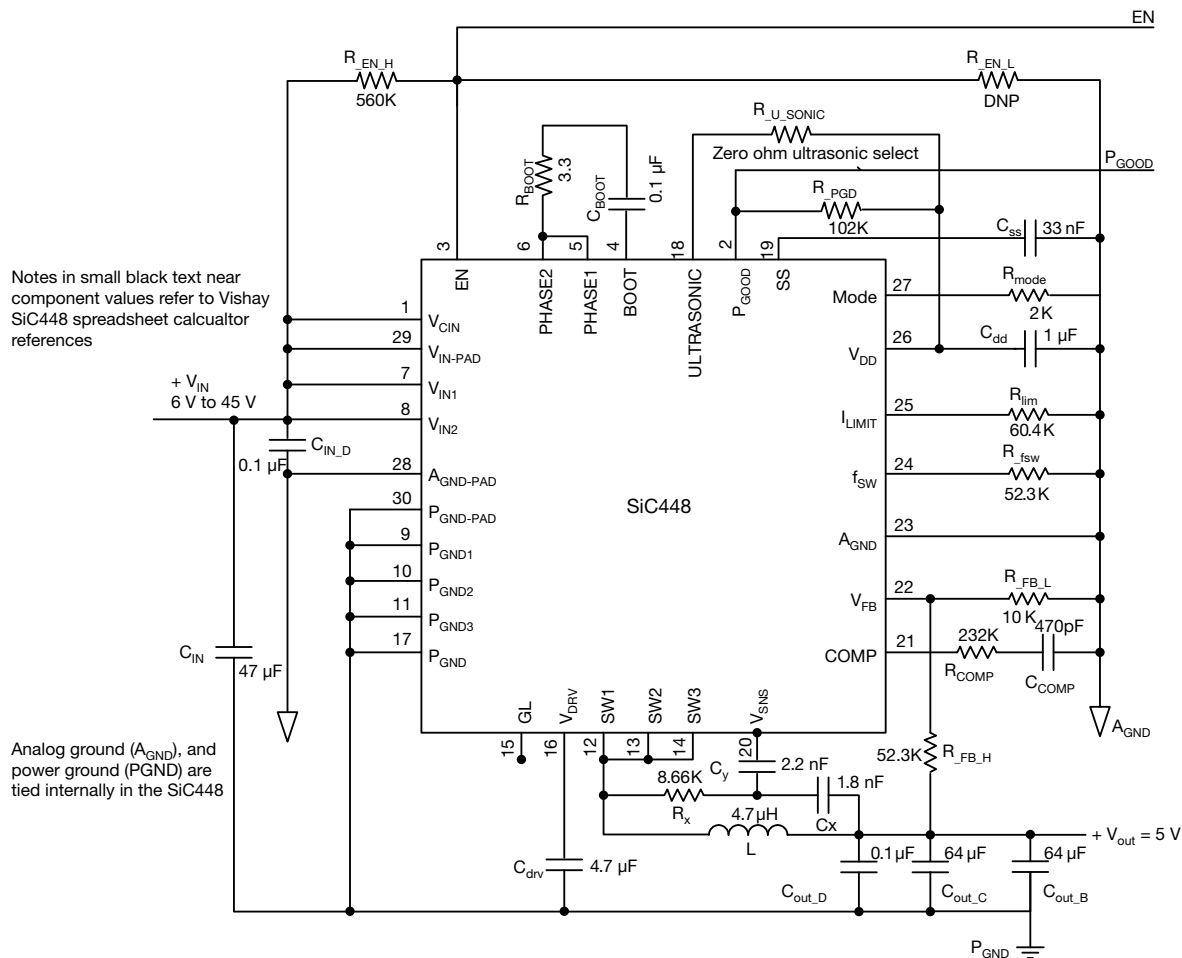
**Power Good**

The SiC448's power good is an open-drain output. Pull P<sub>GOOD</sub> pin high through a > 10 k $\Omega$  resistor to use this signal. The power good window is shown in Fig. 9. If voltage on FB pin is out of this window, the P<sub>GOOD</sub> signal is de-asserted by pulling down to A<sub>GND</sub>. To prevent false triggering during transient events, P<sub>GOOD</sub> has a 25  $\mu$ s blanking time.



**Fig. 9 - P<sub>GOOD</sub> Window**

### EXAMPLE SCHEMATIC



**Fig. 10 - Configured for 6 V to 45 V Input, 5 V Output at 6 A, 500 kHz Operation with Ultrasonic Power Save Mode Enabled  
all Ceramic Output Capacitance Design**

## EXTERNAL COMPONENT SELECTION

This section explains external component selection for the SiC448. Component reference designators in any equation refer to the schematic shown in Fig. 10.

### Output Voltage Adjustment

If a different output voltage is needed, simply change the value of  $V_{OUT}$  and solve for  $R_{FB\_H}$  based on the following formula:

$$R_{FB\_H} = \frac{R_{FB\_L}(V_{OUT} - V_{FB})}{V_{FB}}$$

where  $V_{FB}$  is 0.8 V.  $R_{FB\_L}$  should be a maximum of 10 k $\Omega$  to prevent  $V_{OUT}$  from drifting at no load.

### Switching Frequency Selection

The following equation illustrates the relationship between frequency,  $V_{IN}$ ,  $V_{OUT}$ , and  $R_{fsw}$  value:

$$R_{fsw} = \frac{V_{OUT}}{f_{sw} \times (190 \times 10^{-12})}$$

### Inductor Selection

In order to determine the inductance, the ripple current must first be defined. Low inductor values allow for the use of smaller package sizes but create higher ripple current which can reduce efficiency. Higher inductor values will reduce the ripple current and, for a given DC resistance, are more efficient. However, larger inductance translates directly into larger packages and higher cost. Cost, size, output ripple, and efficiency are all used in the selection process.

The ripple current will also set the boundary for power save operation. The SiC448 will typically enter power save mode when the load current decreases to 1/2 of the ripple current. For example, if ripple current is 1.8 A, power save operation will be active for loads less than 0.9 A. If ripple current is set at 30 % of maximum load current, power save will typically start at a load which is 15 % of maximum current.

The inductor value is typically selected to provide ripple current of 25 % to 50 % of the maximum load current. This provides an optimal trade-off between cost, efficiency, and transient performance. During the on-time, voltage across the inductor is  $(V_{IN} - V_{OUT})$ . The equations for determining inductance are shown below.

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{sw}}$$

and

$$L = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{I_{OUT\_MAX} \times K}$$

where, K is the maximum percentage of ripple current. The designer can quickly make a choice of inductor if the ripple percentage is decided, usually no more than 30 % however higher or lower percentages of  $I_{OUT}$  can be acceptable depending on application. This device allows choices larger than 30 %.

Other than the inductance the DCR and saturation current parameters are key values. The DCR causes an  $I^2R$  loss which will decrease the system efficiency and generate heat. The saturation current has to be higher than the maximum output current plus 1/2 of the ripple current. In an overcurrent condition the inductor current may be very high. All this needs to be considered when selecting the inductor.

### Output Capacitor Selection

The SiC448 is stable with any type of output capacitors by choosing the appropriate  $V_{RAMP}$  components. This allows the user to choose the output capacitance based on the best trade off of board space, cost and application requirements.

The output capacitors are chosen based upon required ESR and capacitance. The maximum ESR requirement is controlled by the output ripple voltage requirement and the DC tolerance. The output voltage has a DC value that is equal to the valley of the output ripple plus half of the peak-to-peak ripple. A change in the output ripple voltage will lead to a change in DC voltage at the output. The relationship between output voltage ripple, output capacitance and ESR of the output capacitor is shown by the following equation:

$$V_{RIPPLE} = I_{RIPPLE(MAX.)} \times \left( \frac{1}{8 \times C_o \times f_{sw}} + ESR \right) \quad (1)$$

Where  $V_{RIPPLE}$  is the maximum allowed output ripple voltage;  $I_{RIPPLE(MAX.)}$  is the maximum inductor ripple current;  $f_{sw}$  is the switching frequency of the converter;  $C_o$  is the total output capacitance; ESR is the equivalent series resistance of the total output capacitors.

In addition to the output ripple voltage requirement, the output capacitors need to meet transient requirements. A worst case load release condition (from maximum load to no load at the exact moment when inductor current is at the peak) determines the required capacitance. If the load release is instantaneous (load changes from maximum to zero within 1  $\mu$ s), the output capacitor must absorb all the energy stored in the inductor. The peak voltage on the capacitor,  $V_{PK}$ , under this worst case condition can be calculated by following equation:

$$C_{OUT\_MIN.} = \frac{L \times \left( I_{OUT} + \frac{1}{2} \times I_{RIPPLE(MAX.)} \right)^2}{(V_{PK})^2 - (V_{OUT})^2} \quad (2)$$

During the load release time, the voltage across the inductor is approximately  $-V_{OUT}$ . This causes a down-slope or falling  $di/dt$  in the inductor. If the load  $di/dt$  is not much faster than the  $di/dt$  of the inductor, then the inductor current will tend to track the falling load current. This will reduce the excess inductive energy that must be absorbed by the output capacitor; therefore a smaller capacitance can be used. The following can be used to calculate the required capacitance for a given  $di_{LOAD}/dt$ .



Peak inductor current,  $I_{LPK}$ , is shown by the next equation:

$$I_{LPK} = I_{MAX.} + \frac{1}{2} \times I_{RIPPLE(MAX.)}$$

The slew rate of load current =  $\frac{di_{LOAD}}{dt}$

$$C_{OUT\_MIN.} = I_{LPK} \times \frac{L \times \frac{I_{LPK}}{V_{OUT}} - \frac{I_{MAX.}}{\frac{di_{LOAD}}{dt}} \times dt}{2(V_{PK} - V_{OUT})} \quad (3)$$

Based on application requirement, either equation (2) or equation (3) can be used to calculate the ideal output capacitance to meet transition requirement. Compare this calculated capacitance with the result from equation (1) and choose the larger value to meet both ripple and transition requirement.

#### Enable Pin Voltage

The EN pin has an internal 5 M $\Omega$  pull down resistor connected to A<sub>GND</sub>. In order to enable the device, an external signal greater than 1.4 V is required. The enable can also be used to set the minimum  $V_{CIN}$ ,  $V_{IN}$  startup voltage by connecting a voltage divider between  $V_{IN}$ , EN, and P<sub>GND</sub>. An automated calculator is available to assist in component selection.

#### Current Limit Resistor

The current limit is set by placing a resistor between  $I_{LIM}$  and A<sub>GND</sub>. The values can be found using the following equation:

$$R_{LIM} (k\Omega) = \frac{K_{LIM}}{I_{OUT\_MAX.} - \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times f_{sw} \times V_{IN} \times L}}$$

Where

- $I_{OUT\_MAX.}$  is desired DC current limit level
- $K_{LIM}$  is determined by Table 2

**TABLE 2 -  $K_{LIM}$  VALUE**

PART NUMBER	$K_{LIM}$
SiC448	420K

#### Note

- It is suggested that the current limit setting not be higher than 2 times the rated current of the part. Be sure max. current limit is within the saturation current of the inductor

#### Input Capacitance

In order to determine the minimum capacitance the input voltage ripple needs to be specified;  $V_{IN\_PK-PK} \leq 500$  mV is a suitable starting point. This magnitude is determined by the final application specification. The input current needs to be determined for the lowest operating input voltage,

$$I_{VCIN(RMS)} = I_O \times \sqrt{D \times (1 - D) + \frac{1}{12} \times \left( \frac{V_{OUT}}{L \times f_{sw} \times I_{OUT}} \right)^2 \times (1 - D)^2 \times D}$$

The minimum input capacitance can then be found,

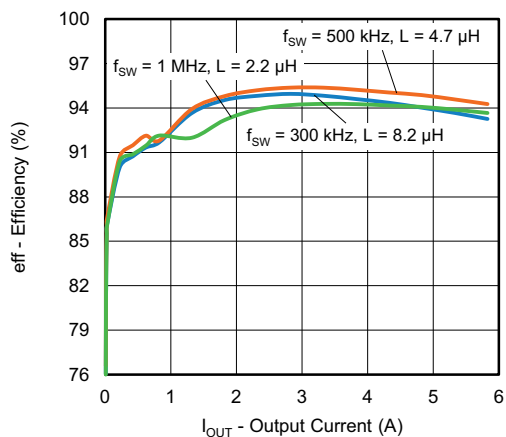
$$C_{VIN\_MIN.} = I_{OUT} \times \frac{D \times (1 - D)}{V_{IN\_PK-PK} \times f_{sw}}$$

If high ESR capacitors are used, it is good practice to also add low ESR ceramic capacitance. A 4.7  $\mu$ F ceramic input capacitance is a suitable starting point.

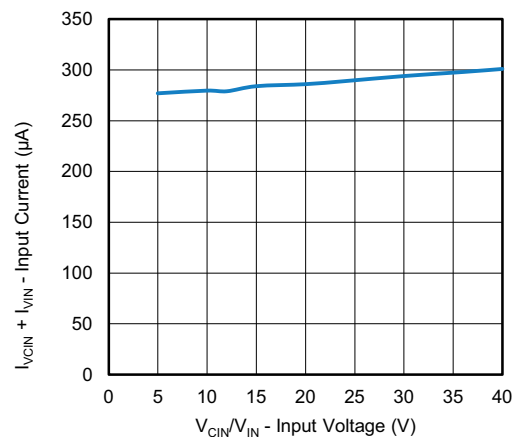
Note, account for voltage derating of capacitance when using all ceramic input capacitors.

# ELECTRICAL CHARACTERISTICS

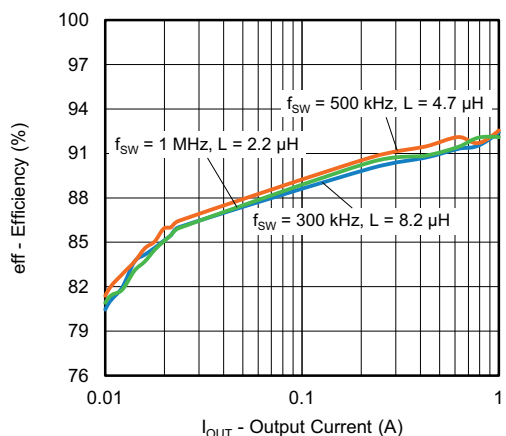
( $V_{IN} = 24\text{ V}$ ,  $V_{OUT} = 5\text{ V}$ ,  $f_{SW} = 300\text{ kHz}$ ,  $L_O = 8.2\text{ }\mu\text{H}$  (IHLP5050FDER8R2M01) unless otherwise noted)



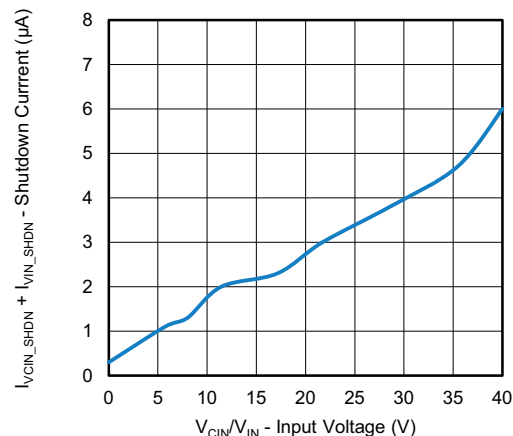
**Fig. 11 - Efficiency, Load 0 A to 6 A**



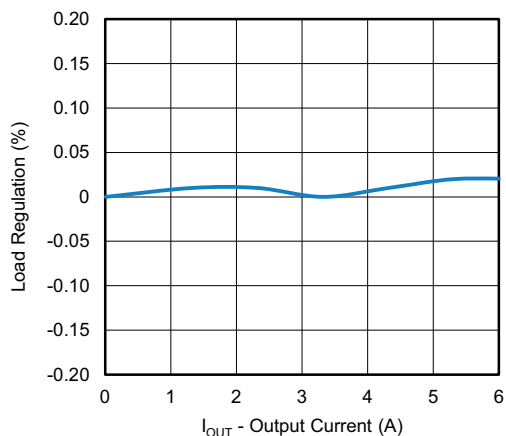
**Fig. 14 - Input Current vs. Input Voltage**



**Fig. 12 - Light Load Efficiency, Load < 1 A**



**Fig. 15 - Input Current vs. Input Voltage**



**Fig. 13 - Load Regulation**

# ELECTRICAL CHARACTERISTICS

( $V_{IN} = 24\text{ V}$ ,  $V_{OUT} = 5\text{ V}$ ,  $f_{sw} = 300\text{ kHz}$ ,  $L_O = 8.2\text{ }\mu\text{H}$  (IHLP5050FDER8R2M01) unless otherwise noted)

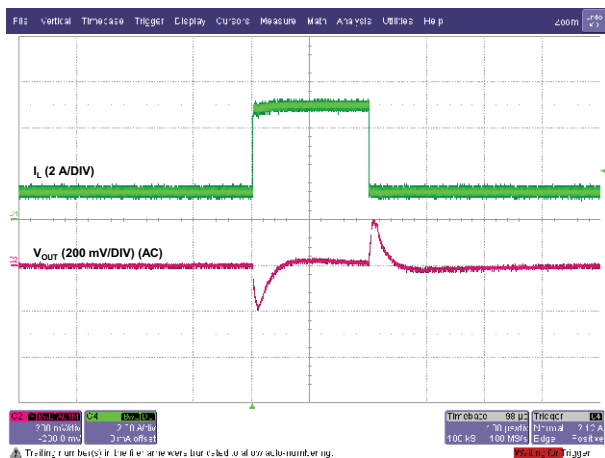


Fig. 16 - Transient Load, Load = 20% to 80%

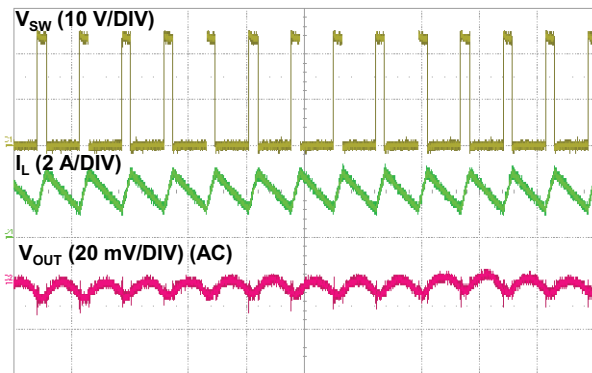


Fig. 19 - Output Ripple, Load = 2 A

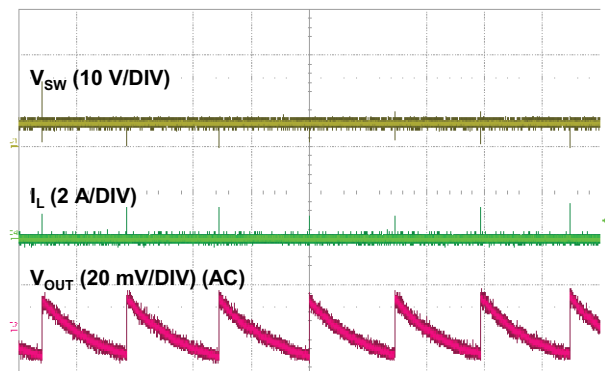


Fig. 17 - Output Ripple, Load = 0 A

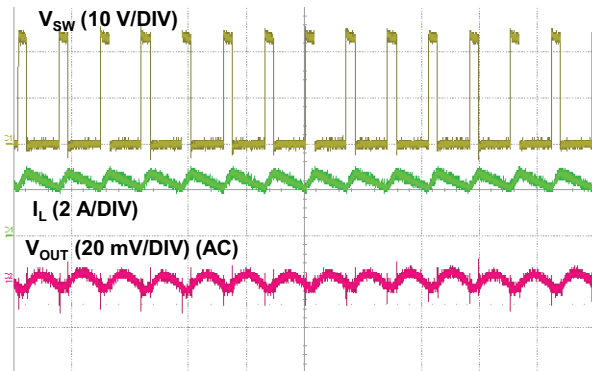


Fig. 20 - Output Ripple, Load = 6 A

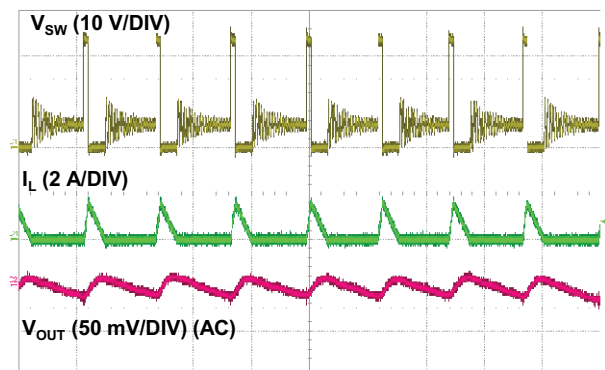


Fig. 18 - Output Ripple, Load = 0.2 A

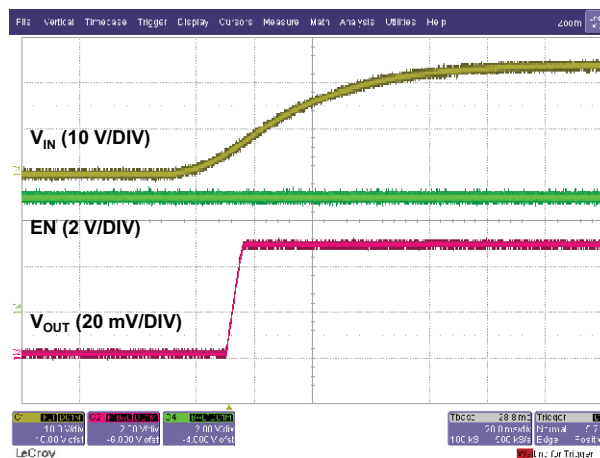
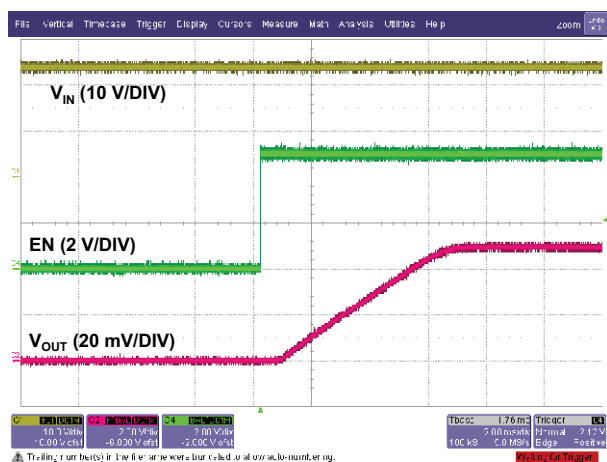
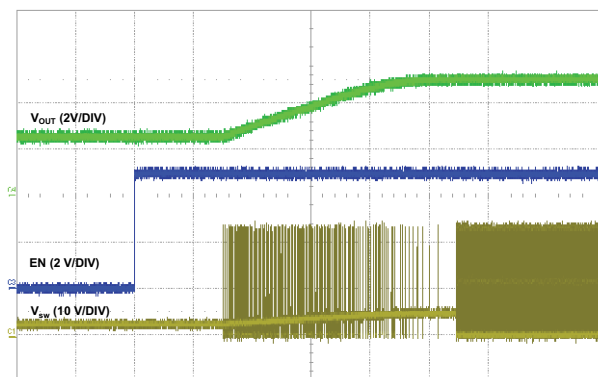


Fig. 21 - Start Up With  $V_{IN}$

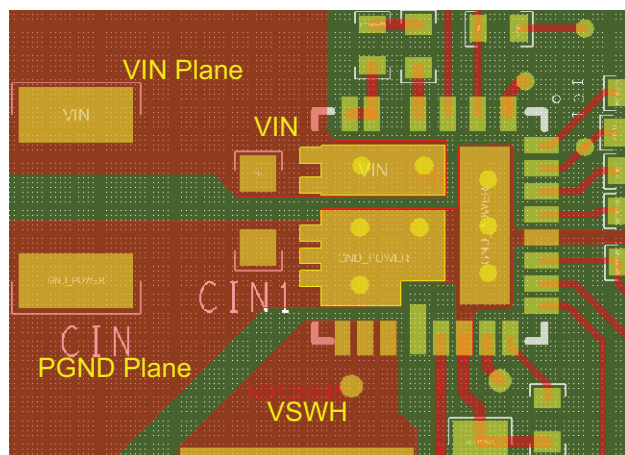



**Fig. 22 - Start Up With Enable**

**Fig. 23 -  $V_{OUT}$  Pre-Biased Start Up**



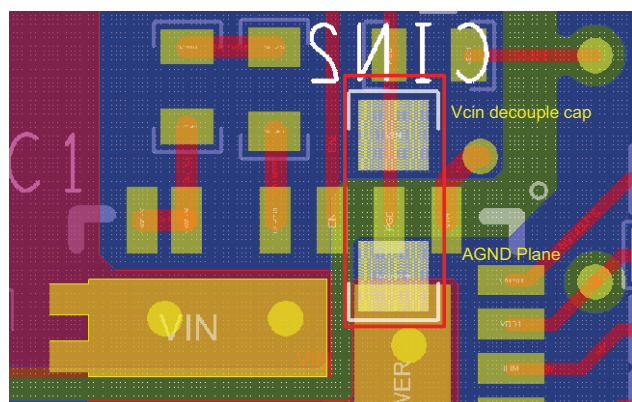
## PCB LAYOUT RECOMMENDATIONS

### Step 1: $V_{IN}$ /GND Planes and Decoupling


**Fig. 24**

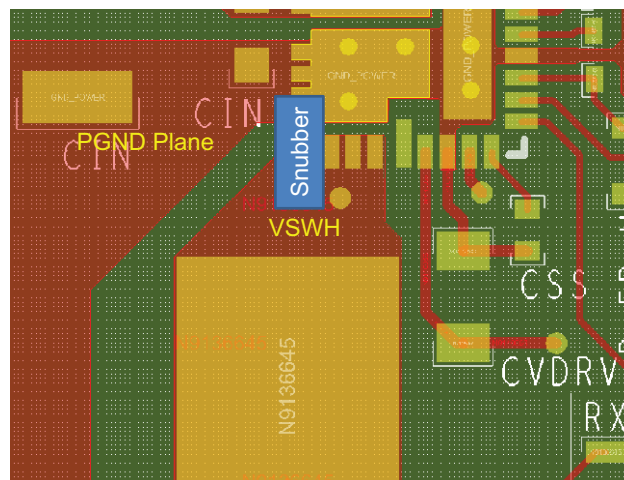
1. Layout  $V_{IN}$  and  $P_{GND}$  planes as shown above
2. Ceramic capacitors should be placed between  $V_{IN}$  and  $P_{GND}$ , and very close to the device for best decoupling effect
3. Various ceramic capacitor values and package sizes should be used to cover entire coupling spectrum e.g. 1210 and 0603
4. Smaller capacitance values, closer to  $V_{IN}$  pin(s), provide better high frequency response

### Step 2: $V_{CIN}$ Pin


**Fig. 25**

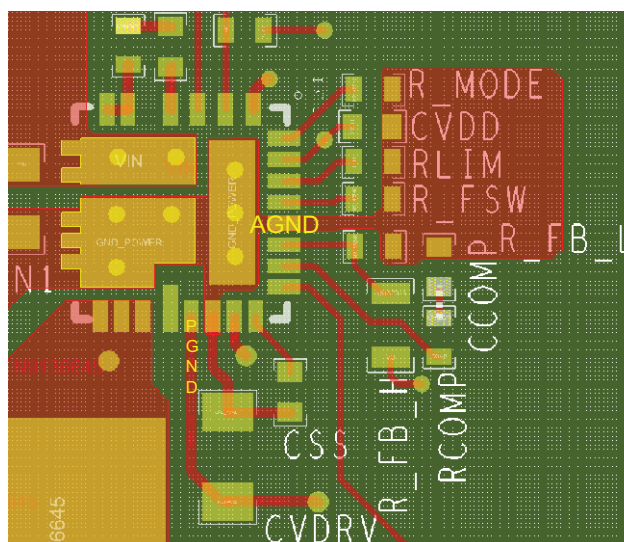
1.  $V_{CIN}$  is the input pin for both internal LDO and  $t_{ON}$  block.  $t_{ON}$  varies with input voltage and it is necessary to put a decoupling capacitor close to this pin
2. The connection can be made through a via and the capacitor can be placed at bottom layer

### Step 3: SW Plane

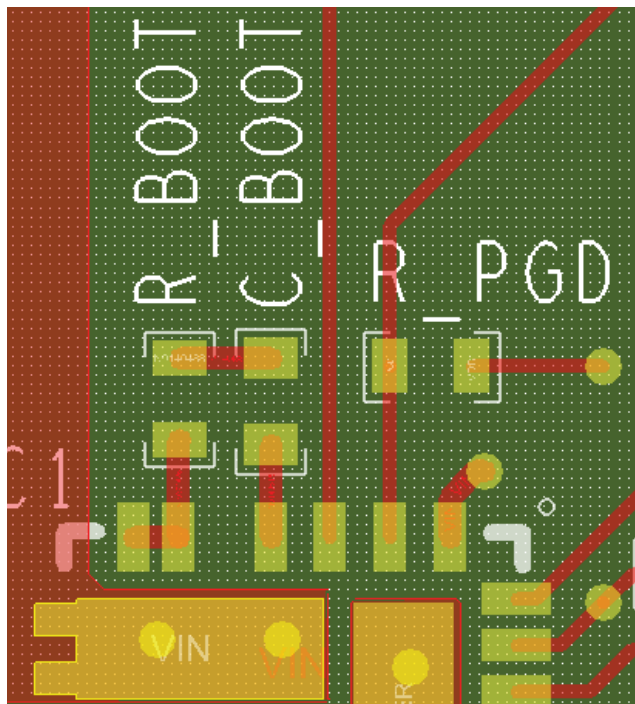

**Fig. 26**

1. Connect output inductor to device with large plane to lower resistance
2. If any snubber network is required, place the components on the bottom side as shown above

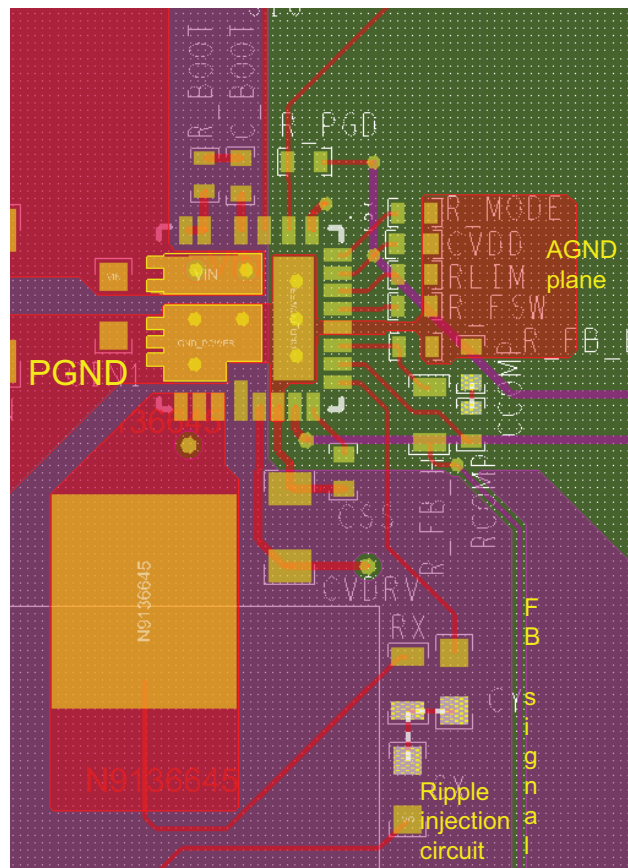
### Step 4: $V_{DD}/V_{DRV}$ Input Filter


**Fig. 27**

1.  $C_{VDD}$  cap should be placed between  $V_{DD}$  and  $A_{GND}$  to achieve best noise filtering
2.  $C_{VDRV}$  cap should be placed close to  $V_{DRV}$  and  $P_{GND}$  pins to reduce effects of trace impedance and provide maximum instantaneous driver current for low side MOSFET during switching cycle

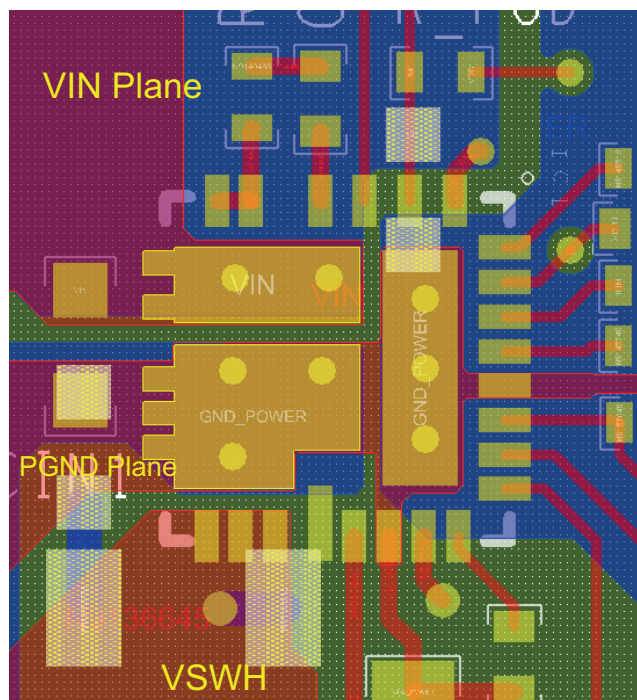
**Step 5: BOOT Resistor and Capacitor Placement**

**Fig. 28**

1.  $C_{BOOT}$  and  $R_{BOOT}$  need to be placed very close to the device, between PHASE and BOOT pins
2. In order to reduce parasitic inductance, it is recommended to use 0402 chip size for the resistor and the capacitor

**Step 6: Signal Routing**

**Fig. 29**

1. Separate the small analog signal from high current path. As shown above, the high current paths with high  $dv/dt$ ,  $di/dt$  are placed on the left side of the IC, while the small control signals are placed on the right side of the IC. All the components for small analog signal should be placed closer to IC with minimum trace length
2. IC analog ground ( $A_{GND}$ ), pin 23, should have a single connection to  $P_{GND}$ . The  $A_{GND}$  ground plane connected to pin 23 helps to keep  $A_{GND}$  quiet and improves noise immunity
3. Feedback signal can be routed through inner layer. Make sure this signal is far from SW node and shielded by inner ground layer
4. Ripple injection circuit can be placed next to inductor. Kelvin connection as shown above is recommended

### Step 7: Adding Thermal Relief Vias and Duplicate Power Path Plane

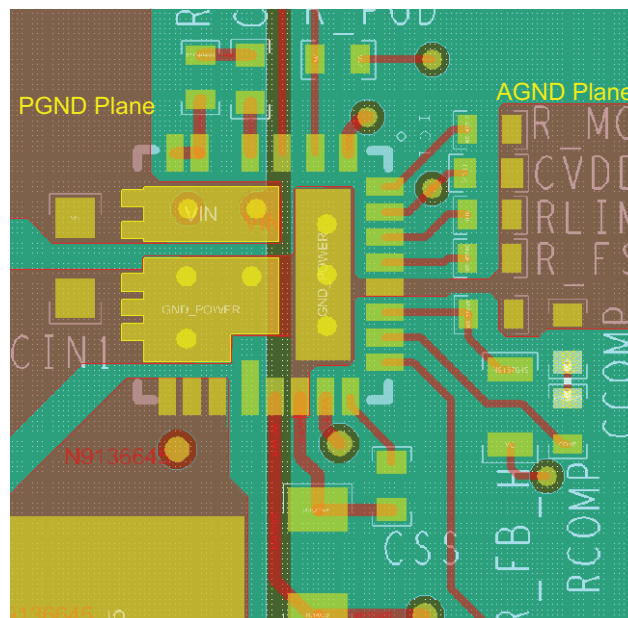


**Fig. 30**

1. Thermal relief vias can be added on the  $V_{IN}$  and  $P_{GND}$  pads to utilize inner layers for high current and thermal dissipation
2. To achieve better thermal performance, additional vias can be placed on  $V_{IN}$  and  $P_{GND}$  planes. It is also necessary to duplicate the  $V_{IN}$  and ground plane at bottom layer to maximize the power dissipation capability of the PCB
3. SW pad is a noise source and it is not recommended to place vias on this pad
4. 8 mil vias on pads and 10 mil vias on planes are ideal via sizes. The vias on pad may drain solder during assembly

and cause assembly issues. Please consult with the assembly house for guideline

### Step 8: Ground Layer



**Fig. 31**

1. It is recommended to make the entire inner layer (next to top layer) ground plane
2. This ground plane provides shielding between noise source on top layer and signal trace within inner layer
3. The ground plane can be broken into two sections,  $P_{GND}$  and  $A_{GND}$

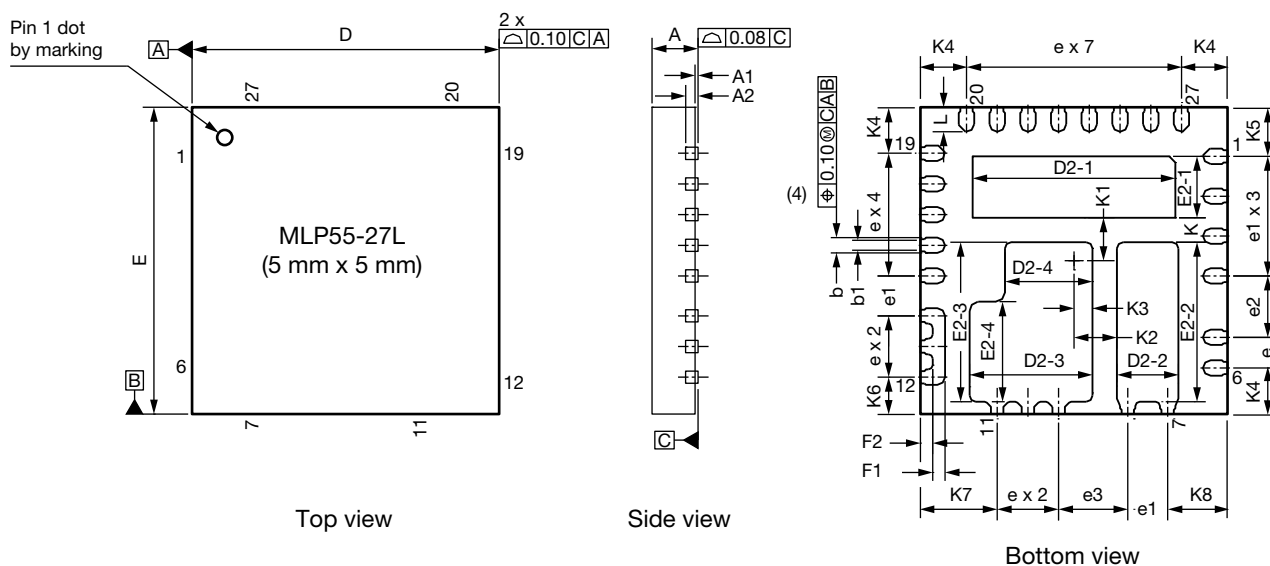


PRODUCT SUMMARY	
Part number	SiC448
Description	6 A, 4.5 V to 45 V input, 100 kHz to 2 MHz, synchronous buck regulator
Input voltage min. (V)	4.5
Input voltage max. (V)	45
Output voltage min. (V)	0.8
Output voltage max. (V)	$0.92 \times V_{IN}$
Continuous current (A)	6
Switch frequency min. (kHz)	100
Switch frequency max. (kHz)	2000
Pre-bias operation (yes / no)	Yes
Internal bias reg. (yes / no)	Yes
Compensation	External
Enable (yes / no)	Yes
P <sub>GOOD</sub> (yes / no)	Yes
Overcurrent protection	Yes
Protection	OVP, OCP, UVP/SCP, OTP, UVLO
Light load mode	Selectable powersave / ultrasonic
Peak efficiency (%)	98
Package type	PowerPAK MLP55-27L
Package size (W, L, H) (mm)	5 x 5 x 0.75
Status code	1
Product type	microBUCK (step down regulator)
Applications	Computing, consumer, industrial, healthcare, networking

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?77185](http://www.vishay.com/ppg?77185).



## PowerPAK® MLP55-27 Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A <sup>(8)</sup>	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2	0.20 ref.			0.008 ref.		
b <sup>(4)</sup>	0.20	0.25	0.30	0.008	0.010	0.012
b1	0.15	0.20	0.25	0.006	0.008	0.010
D	5.00 BSC			0.197 BSC		
e	0.50 BSC			0.020 BSC		
e1	0.65 BSC			0.026 BSC		
e2	1.00 BSC			0.039 BSC		
e3	1.13 BSC			0.044 BSC		
E	5.00 BSC			0.197 BSC		
L	0.35	0.40	0.45	0.014	0.016	0.018
N <sup>(3)</sup>	28			28		
D2-1	3.25	3.30	3.35	0.128	0.130	0.132
D2-2	0.95	1.00	1.05	0.037	0.039	0.041
D2-3	1.95	2.00	2.05	0.077	0.079	0.081
D2-4	1.37	1.42	1.47	0.054	0.056	0.058
E2-1	0.95	1.00	1.05	0.037	0.039	0.041
E2-2	2.55	2.60	2.65	0.100	0.102	0.104
E2-3	2.55	2.60	2.65	0.100	0.102	0.104
E2-4	1.58	1.63	1.68	0.062	0.064	0.066
F1	0.20	-	0.25	0.008	-	0.010
F2	min. 0.20			min. 0.008		



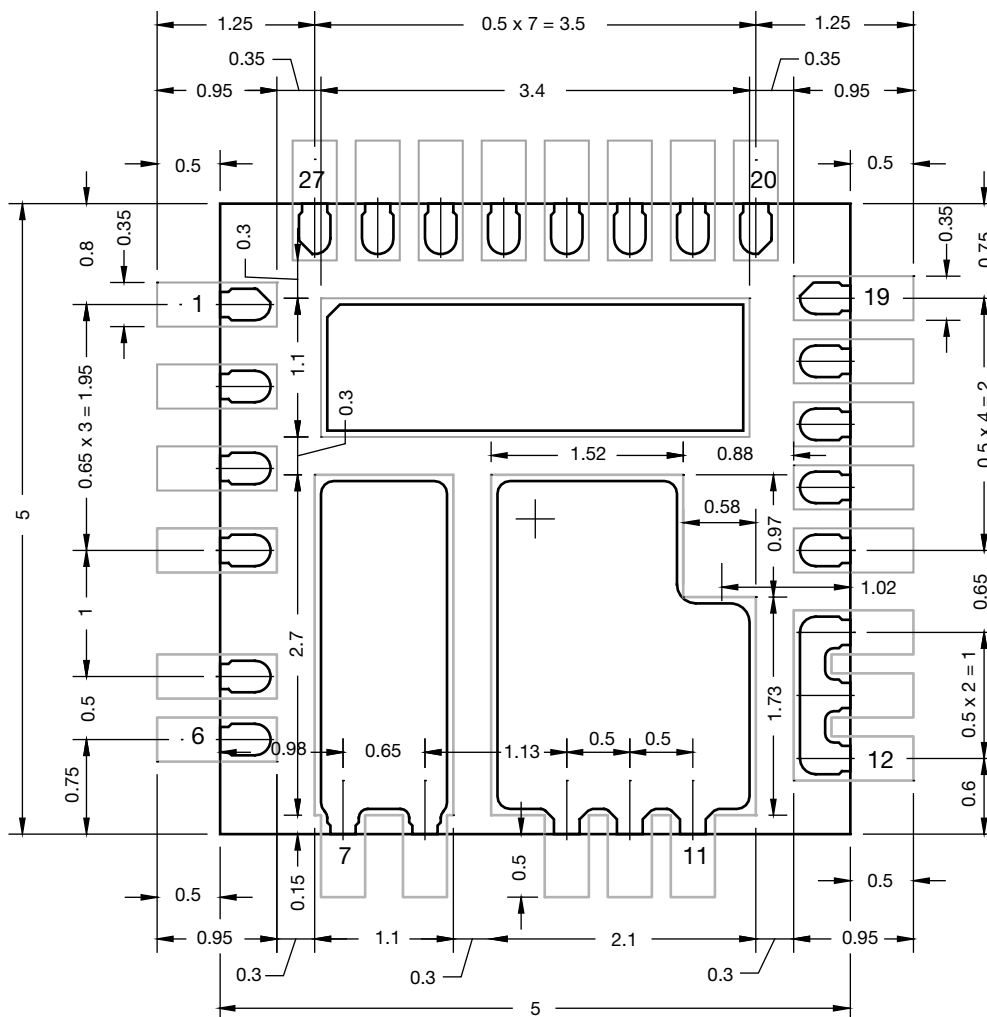
DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
K	0.40 BSC			0.016 BSC		
K1	0.70 BSC			0.028 BSC		
K2	0.70 BSC			0.028 BSC		
K3	0.30 BSC			0.012 BSC		
K4	0.75 BSC			0.030 BSC		
K5	0.80 BSC			0.0315 BSC		
K6	0.60 BSC			0.024 BSC		
K7	1.25 BSC			0.049 BSC		
K8	0.975 BSC			0.038 BSC		
ECN: T18-0594-Rev. C, 03-Dec-2018 DWG: 6056						

**Notes**

- (1) Use millimeters as the primary measurement
- (2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994
- (3) N is the number of terminals  
Nd is the number of terminals in x-direction  
Ne is the number of terminals in y-direction
- (4) Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
- (5) The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
- (6) Exact shape and size of this feature is optional
- (7) Package warpage max. 0.08 mm
- (8) Applied only for terminals

## Recommended Land Pattern

### PowerPAK® MLP55-27L



All dimensions in millimeters



Component for MLP55-27L



Land pattern for MLP55-27L





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