Dual N-Channel 25 V (D-S) MOSFETs

DESCRIPTION

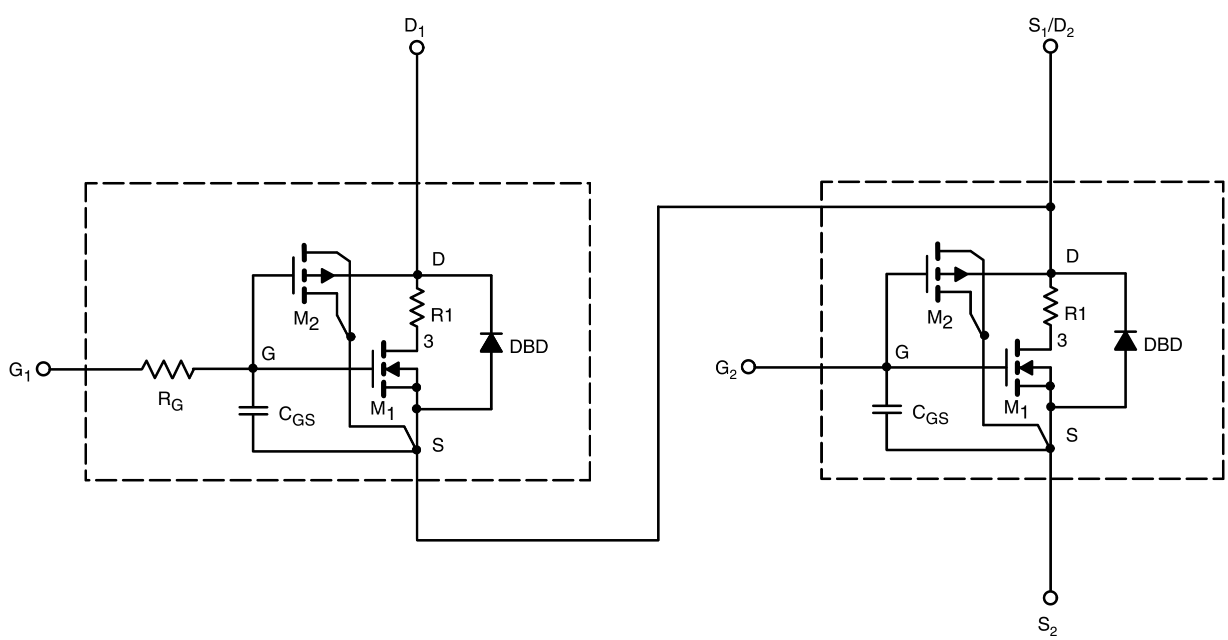
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over the -55 °C to +125 °C temperature range
- Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**SIMULATED DATA**	**MEASURED DATA**	**UNIT**
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	Ch-1	1.7	-	V
			Ch-2	1.7	-	
Drain-Source On-State Resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 5 A	Ch-1	0.00390	0.00380	Ω
		V_{GS} = 10 V, I_D = 8 A	Ch-2	0.00179	0.00173	
		V_{GS} = 4.5 V, I_D = 3 A	Ch-1	0.00660	0.00640	
		V_{GS} = 4.5 V, I_D = 5 A	Ch-2	0.00281	0.00265	
Forward Transconductance [a]	g_{fs}	V_{DS} = 10 V, I_D = 5 A	Ch-1	29	40	S
		V_{DS} = 10 V, I_D = 8 A	Ch-2	57	55	
Diode Forward Voltage [b]	V_{SD}	I_S = 5 A, V_{GS} = 0 V	Ch-1	0.80	0.81	V
		I_S = 8 A, V_{GS} = 0 V	Ch-2	0.77	0.77	
Dynamic [b]						
Input Capacitance	C_{iss}	Channel-1 V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz; Channel-2 V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	Ch-1	931	925	pF
			Ch-2	2160	2150	
Output Capacitance	C_{oss}		Ch-1	321	310	
			Ch-2	779	800	
Reverse Transfer Capacitance	C_{rss}		Ch-1	58	52	
			Ch-2	87	100	
Total Gate Charge	Q_g	Channel-1 V_{DS} = 10 V, V_{GS} = 10 V, I_D = 5 A; Channel-2 V_{DS} = 10 V, V_{GS} = 10 V, I_D = 8 A	Ch-1	12.1	12.5	nC
			Ch-2	27	27	
		Channel-1 V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 5 A; Channel-2 V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 8 A	Ch-1	5.6	5.9	
			Ch-2	12.3	12.5	
Gate-Source Charge	Q_{gs}		Ch-1	2.5	2.5	
			Ch-2	5.4	5.4	
Gate-Drain Charge	Q_{gd}		Ch-1	1.2	1.2	
			Ch-2	2.1	2.1	

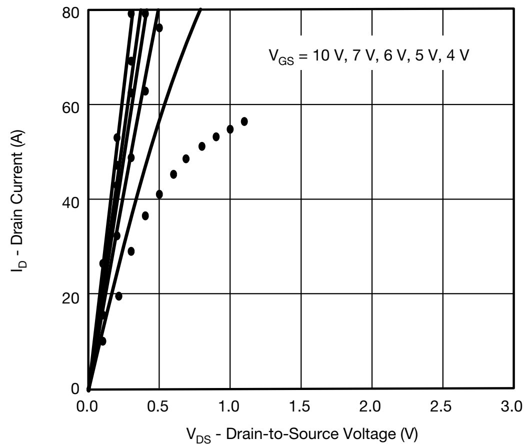
Notes

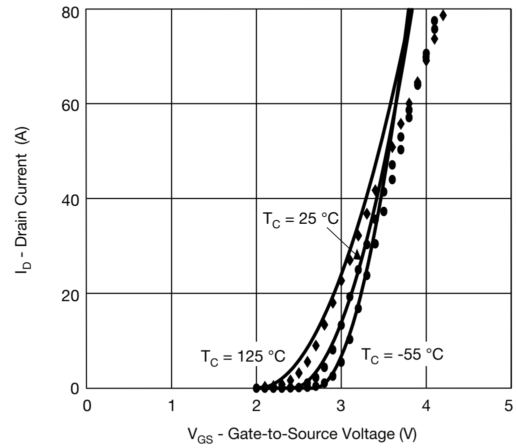
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

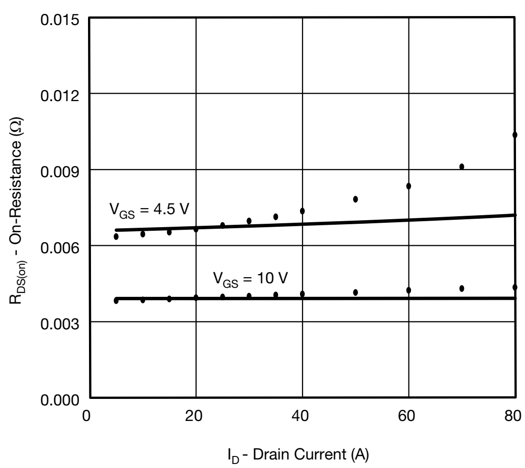
b. Guaranteed by design, not subject to production testing

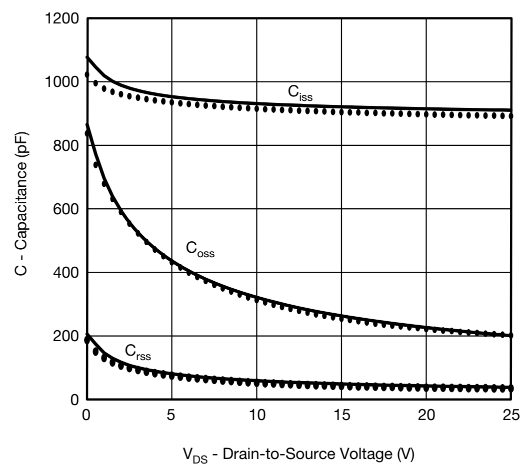
COMPARISON OF MODEL WITH MEASURED DATA T_J = 25 °C, unless otherwise noted

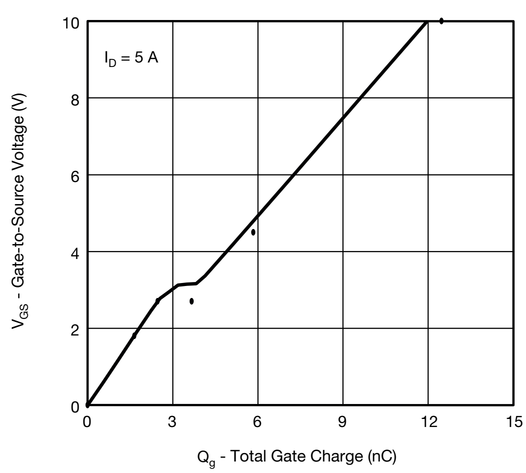
N-Channel 1 MOSFET

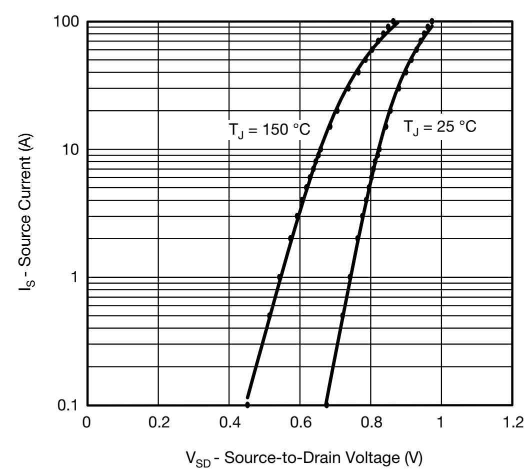










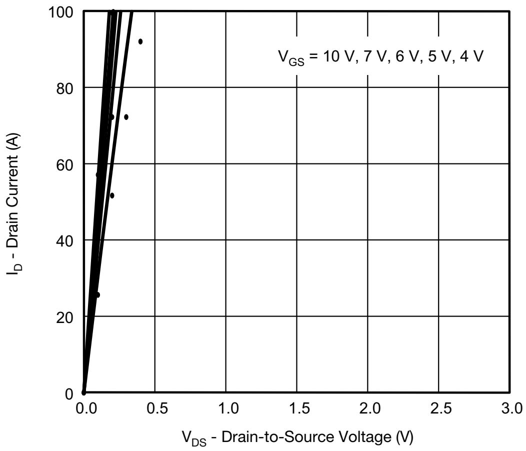


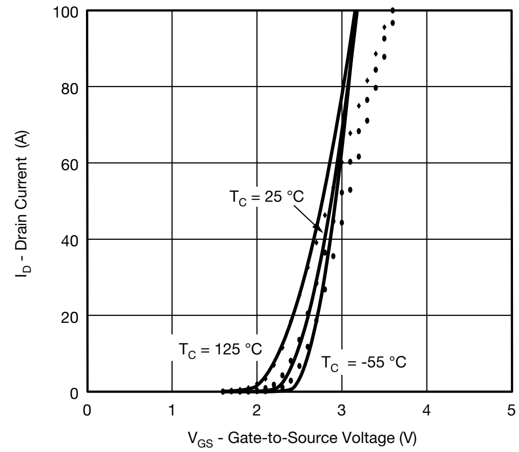
Note

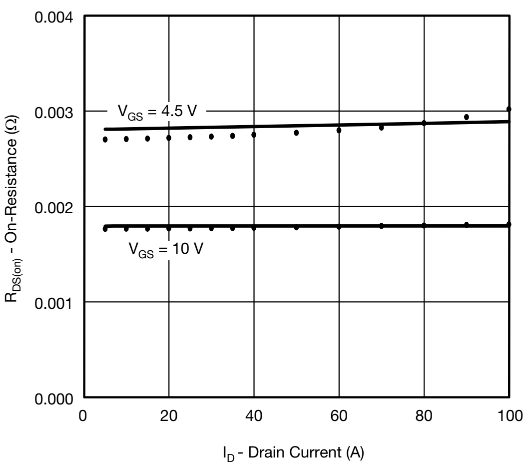
- Dots and squares represent measured data

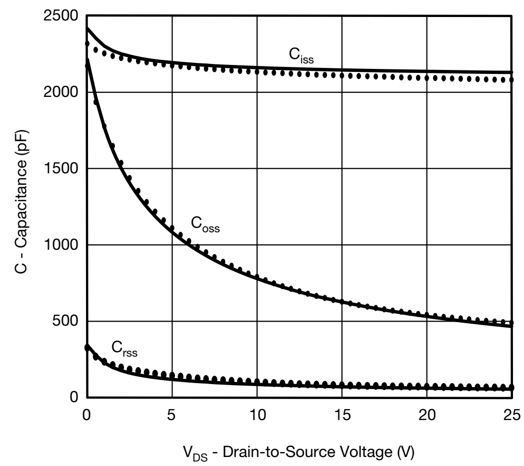
COMPARISON OF MODEL WITH MEASURED DATA T_J = 25 °C, unless otherwise noted

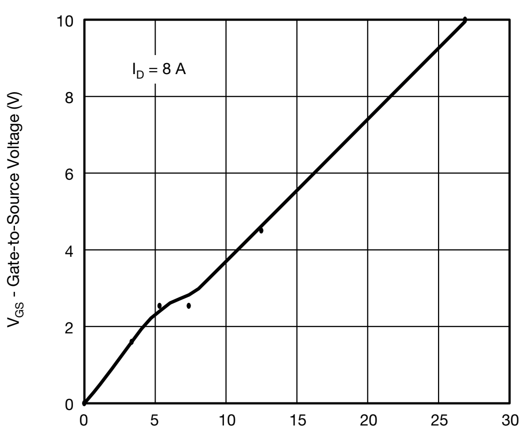
N-Channel 2 MOSFET

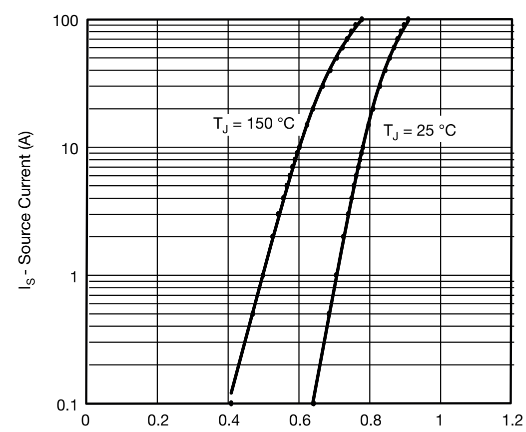












Note

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