Infrared Emitters and Detectors | Application Note

Designing With the VSMA Series High Power IREDs

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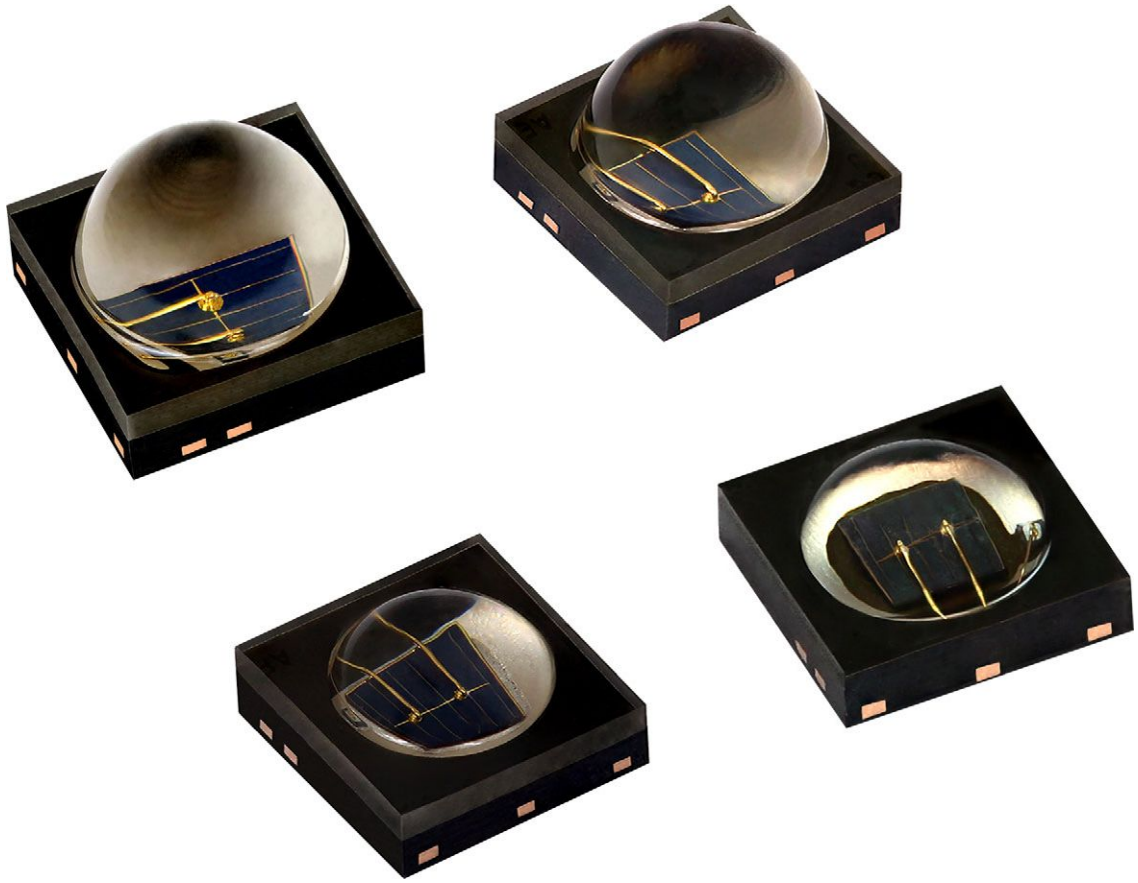

ABSTRACT

This application note provides an overview of the electrical and optical characteristics of Vishay's VSMA high power infrared emitter series. In addition, the basic principles of heat transfer and their influence on the thermal management design for DC and pulsed operation are discussed.

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APPLICATION NOTE

Designing With the VSMA Series High Power IREDs

CONTENTS

Designing With the VSMA Series High Power IREDs

1. INTRODUCTION

Infrared light-emitting diodes (IREDs) are widely used in many application areas today, including for illumination in more traditional high power camera-based applications, as well as in more low power applications, such as sensing and data communication. A key factor for their use is their ability to emit a high radiant intensity due to their high current drive capabilities. There is a growing demand for high power IREDs in many applications to fulfill the requirements for high radiant intensity illumination with fewer components. These application examples include driver and occupant monitoring, eye tracking, and illumination for CCTV.

Moving to a high power IRED allows multiple standard IREDs to be replaced with a single device from the VSMA series, producing a high amount of radiant power with fewer components. Therefore, more space can be saved in the end application.

VSMA10xx250/-X02 VSMA10xx400/-X02 VSMA10xx600/-X02 VSMA10xx750/-X02

Fig. 1 - High Power IRED VSMA Series

Vishay offers the VSMA series in wavelengths of 850 nm and 940 nm, matching the sensitivity range of standard silicon photodiodes and phototransistors, as well as CCD and CMOS cameras. In addition, each wavelength option is offered in three emission angles. Table 1 shows the product summary of the VSMA series:

TABLE 1 - PRODUCT SUMMARY FOR THE VSMA SERIES

COMPONENT	I_e (mW/sr) at I_F = 1 A	φ (°)	λ_p (nm)	$\lambda_{centroid}$ (nm)	t_r (ns)
VSMA1085250/-X02	1350	±28	850	845	13
VSMA1085400/-X02	1025	±40	850	845	13
VSMA1085600/-X02	510	±60	850	845	13
VSMA1085750/-X02	360	±75	850	845	13
VSMA1094250/-X02	1350	±28	945	940	10
VSMA1094400/-X02	1025	±40	945	940	10
VSMA1094600/-X02	510	±60	945	940	10
VSMA1094750/-X02	360	±75	945	940	10

While the latest advancements in chip technology have improved conversion efficiency considerably, the heat dissipated in a high power IRED can quickly rise to a level that needs specific consideration. This heat must be dissipated away from the IRED to ensure the maximum allowed junction temperature inside the IRED is not exceeded. Thermal management design is essential in ensuring the high reliability of the IRED's operation and extended lifetime.

Good thermal management design requires an understanding of the following:

- Heat transfer theory
- The thermal resistance network
- Thermal management design for DC operation
- Thermal management design for dynamic pulsed operation

The VSMA1094250X02 has been used as the basis for the examples given in this application note. The examples hold for the entire VSMA series, with the necessary information extracted from the datasheets of the respective VSMA series IREDs.

2. ELECTRICAL CHARACTERISTICS

A driving circuit that generates a sufficient amount of radiant intensity must be implemented for a given application, while also limiting the current to prevent damaging the IRED. When designing the driving circuit, there are two different possibilities for the IRED's operation, which consists of the following:

- Continuous / DC operation
- Pulsed operation

2.1 Basic Characteristics

The operating forward current I_F can be selected based on the radiant intensity I_e requirement of the end application. The information about the relationship between I_F, V_F, and I_e can be found in the basic characteristics table and graphs in the datasheet.

Fig. 2, Fig. 3, Fig. 4, and Table 2 show the above relation and will help you to find the operating point of the IRED. The basic characteristics table and graph examples provided below are for the VSMA1094250X02. The basic characteristics information for other VSMA series IREDs can be found directly from their respective datasheets. Please note that the values are based on typical values from the datasheet. However, using the minimum values to consider the worst-case scenario is also a good design approach.

TABLE 2 - BASIC CHARACTERISTICS FOR THE VSMA1094250X02
(T_{amb} = 25 °C, unless otherwise noted)

PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Forward voltage	I_F = 0.35 A, t_p = 10 ms	V_F	2.1	2.7	3.0	V
	I_F = 1 A, t_p = 100 µs	V_F	2.2	2.9	3.1	V
	I_F = 1.5 A, t_p = 100 µs	V_F	2.6	3.1	3.35	V
	I_F = 5 A, t_p = 100 µs	V_F	2.7	3.8	4.2	V
Radiant intensity (1)	I_F = 0.35 A, t_p = 10 ms	I_e	415	500	670	mW/sr
	I_F = 1 A, t_p = 100 µs	I_e	1120	1350	1800	mW/sr
	I_F = 1.5 A, t_p = 100 µs	I_e	1660	2000	2700	mW/sr
	I_F = 5 A, t_p = 100 µs	I_e	4975	6000	8000	mW/sr
Radiant power	I_F = 1 A, t_p = 100 µs	ϕ_e	-	1450	-	mW
	I_F = 1.5 A, t_p = 100 µs	ϕ_e	-	2125	-	mW
Temperature coefficient of ϕ	I_F = 1 A, t_p = 100 µs	TK_ϕ	-	-0.15	-	%/K

Note

(1) The radiant intensity values have been measured with a tolerance of ± 11 %

Designing With the VSMA Series High Power IREDs

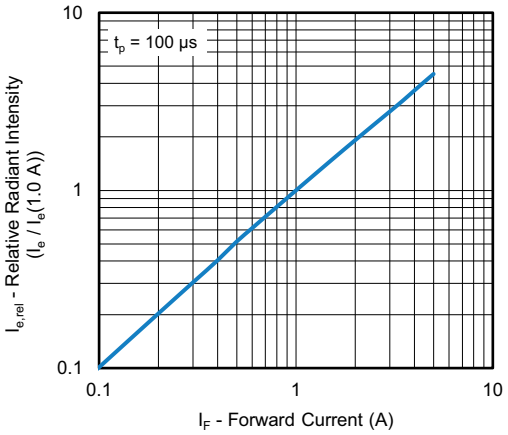

Fig. 2 - Relative Radiant Intensity vs. Forward Current for the VSMA1094250X02

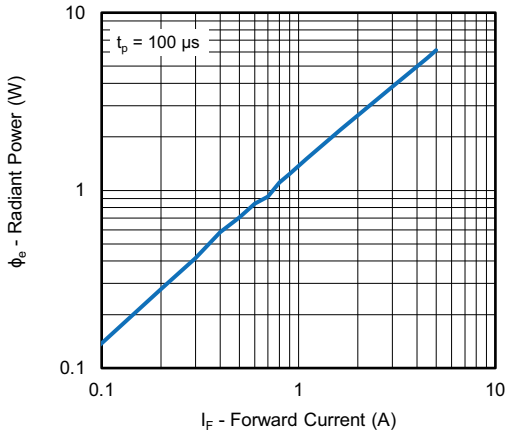

Fig. 3 - Radiant Power vs. Forward Current for the VSMA1094250X02

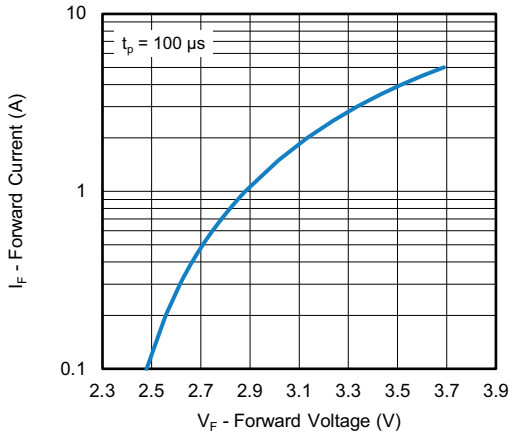

Fig. 4 - Forward Current vs. Forward Voltage for the VSMA1094250X02

APPLICATION NOTE

Designing With the VSMA Series High Power IREDs

2.2 Continuous DC Operation

When the end application requires DC operation and a low I_F, a simple driver circuit can be implemented using a current limiting resistor or a low dropout (LDO) linear voltage regulator to limit the current. These are shown in Fig. 5 and Fig. 6. When a high I_F is required, a more complex current regulator circuit is required to achieve a correct current regulation. One good example is the switching regulator, which is more efficient and allows less power dissipation across the driver circuit.

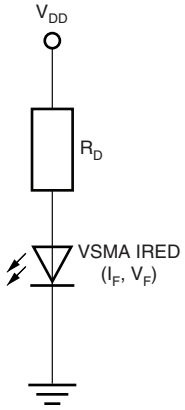

Fig. 5 - Example Circuit With a Current Limiting Resistor

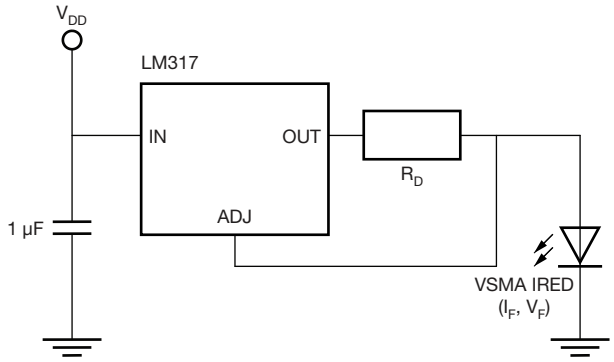

Fig. 6 - Example Circuit With an LM317 Constant Voltage Regulator

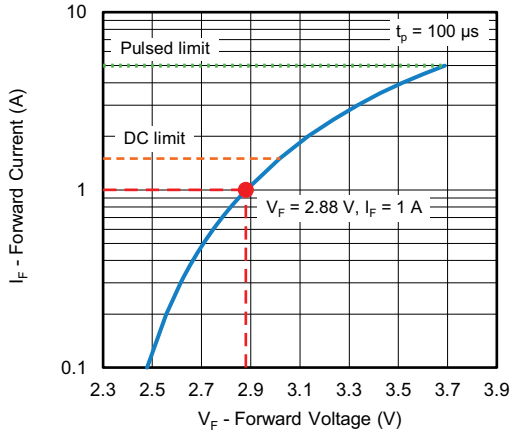

Fig. 7 - DC Operating Point Example
for the VSMA1094250X02

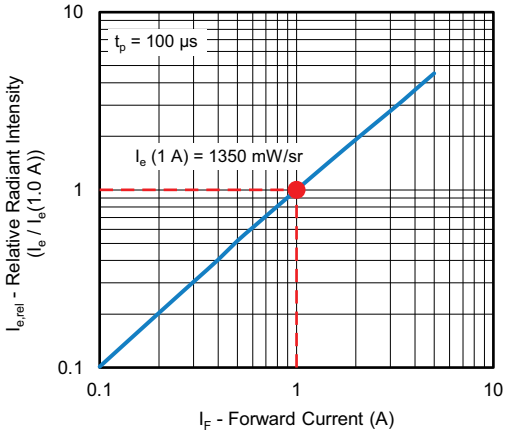

Fig. 8 - Relative Radiant Intensity vs. Forward Current
for the VSMA1094250X02

The operating point of the IRED can be found from the I-V curve. If, for example, the application requires the IRED to be driven at 1 A to achieve a radiant intensity design requirement of 1350 mW/sr, a typical forward voltage of 2.88 V can be derived from the graph in the datasheet, as shown in Fig. 7 and Fig. 8. While designing the application using typical values simplifies the design process, a real-world situation requires designing using minimum I_e and the highest V_F requirements to consider part to part tolerance. This design approach allows the end application to fulfill its design specification at its absolute limit. When using this approach, the radiant intensity in Fig. 8 is I_e, min (1 A) = 1120 mW/sr, whereas the corresponding V_F in Fig. 7 is V_F, max. = 3.1 V. Apart from the radiant intensity, the operating point selection also depends on the capability of the driver circuit used and the thermal management design. The selection of a safe operating point using the DC derating diagram shown in Fig. 23 prevents damaging the IRED and prolongs its lifetime. The topic of the DC derating diagram will be discussed further in Chapter 4.

Example - Current Limiting Series Resistor

The resistor needed for limiting the operating current I_F of the IRED in Fig. 5 can be calculated as follows:

$$R_D = \frac{V_{DD} - V_{F,\,typ.}}{I_F} = \frac{5\ V - 2.7\ V}{0.35\ A} = 6.57\ \Omega$$

With a supply voltage of 5 V, the next closest resistor value from the E12 table to ensure a constant driving current of 0.35 A is approximately 6.8 Ω. This design example is suitable for low driving current and a series connection. However, for higher driving current, a large voltage drop across a series resistor will be inefficient and may cause a heat dissipation problem. Besides that, for a parallel connection, the thermal runaway effect could damage the IRED due to the part to part tolerance of V_F. Therefore, it is recommended to use the constant current regulator for a parallel topology.

Example - Array Connection to Increase Optical Power

When a higher radiant intensity is required for the application, an array connection of the IRED - either in a series or parallel topology - is a viable option. It is recommended to design with a constant regulator to ensure a stable and efficient current source, especially for the higher radiant intensity requirement. Fig. 9 shows an example of the series topology with an LM317 constant voltage regulator.

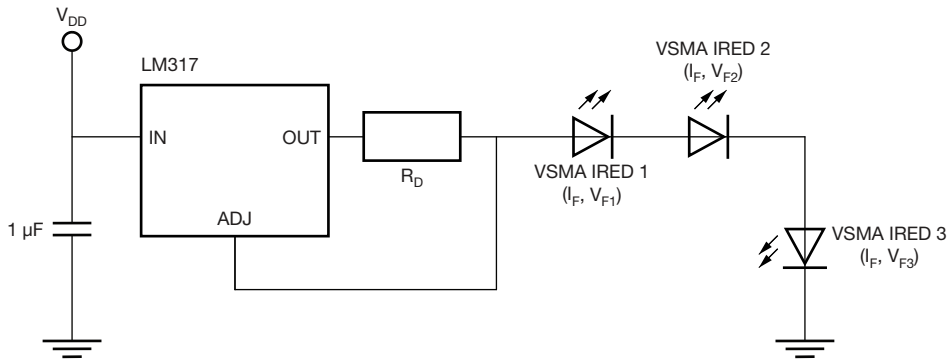

Fig. 9 - Example Circuit in a Series Topology With an LM317 Constant Voltage Regulator

A series topology has the advantage of a simpler circuit design requirement, with only one constant regulator circuit needed. However, it has the disadvantage of a higher voltage supply requirement because the voltage of the IREDs adds up. Besides that, the failure of one IRED causes the failure of the remaining IREDs. Fig. 10 shows an example of the parallel topology.

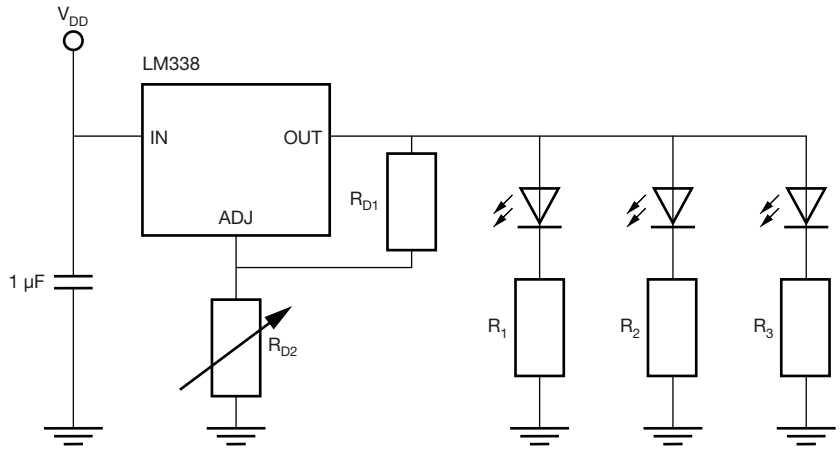

Fig. 10 - Example Circuit in a Parallel Topology With an LM338 Constant Voltage Regulator

A parallel topology has the advantage of redundancy in case one of the IREDs fails. Besides that, the required supply voltage is lower because the voltage of the IREDs does not add up between the branches. However, there is also the challenge of thermal runaway with a parallel topology, where one branch takes the majority of the current because of the lower forward voltage drop when it gets warm. This effect has to be considered by the designer, given that the IRED usually comes with variations in forward voltage drop due to both manufacturing tolerances and temperature effects. However, this effect can be reduced by implementing an individual constant current regulator circuit for each branch.

2.3 Pulsed Operation

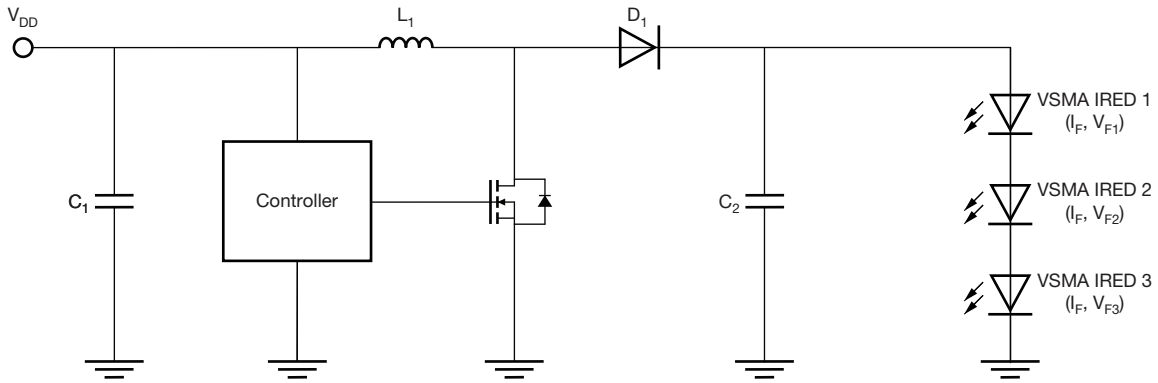

Fig. 11 - Example Circuit With a PWM-Controlled Boost Regulator

Another approach to operating the IRED is periodically or intermittently pulsing the IRED using pulse width modulation (PWM). This allows the operation of the IRED above 1.5 A to avoid surpassing the stated maximum junction temperature and subsequently achieves a higher radiant intensity. For I_F operation below 1.5 A, the pulsed operation would improve the lifetime of the IRED. Together with an efficient switching regulator such as a buck, boost, or buck-boost regulator, the PWM-controlled current driver allows for safe operation of the IRED above the DC limit of 1.5 A. Fig. 11 shows an example circuit with a PWM-controlled boost regulator.

Example - Array Connection With an Individual PWM-Controlled Boost Regulator in Parallel Topology

When a parallel array topology is required to achieve a high radiant intensity IRED, a PWM-controlled boost regulator helps to reduce the thermal runaway effect typically seen in parallel topologies. Such a controller allows an individual current driver with a matching IRED driving current between branches.

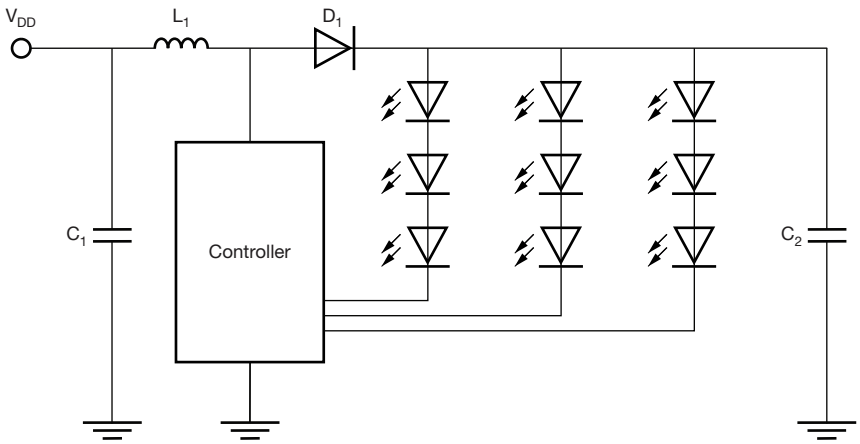

Fig. 12 - Example Circuit in a Parallel Topology With an Individual PWM-Controlled Current Regulator

2.4 Regulated IRED Driver Technologies

It is recommended to drive the IRED with a regulated driver. This is crucial for high power IRED applications where high heat dissipation reduces the lifetime of the IRED. An IRED driver with a current limiting resistor is usually less efficient or could cause thermal runaway in a parallel connection.

There are two main regulated IRED driver technology groups - the linear regulator and the switching regulator. Table 3 shows the difference between linear and switching regulators.

TABLE 3 - DIFFERENT REGULATED IRED DRIVER TECHNOLOGIES

PARAMETER	LINEAR REGULATOR	SWITCHING REGULATOR
Design topology	Low dropout (LDO)	Buck, boost, buck-boost, etc.
Efficiency	Low to medium high	Medium to high
Cost	Low	Medium to high
Input voltage range	Narrow	Wide
EMI / ripple	Low	Medium to high
Application	Low to medium power IRED or / and when the total IRED voltage is just below the supply voltage	High power IRED or / and when the total IRED voltage is higher or significantly lower than the supply voltage

A linear regulator such as an LDO is suitable for powering low to medium powered IREDs where the total IRED voltage is below the supply voltage. There are high output current LDOs in the market. However, the rated output voltage and the input voltage ranges are limited. These will pose a challenge for the array connection of the IRED because it requires a higher supply voltage. Besides that, it is well-known that an LDO is a cheaper solution, but it has a lower efficiency than the switching regulator. A switching regulator can be used for high power IRED applications, where the higher efficiency contributes to lower heat dissipation. This is crucial for extending the lifetime of the IRED. In many applications, there will be a requirement where the total IRED voltage must be higher than the supply voltage. Only the switching regulator could achieve this via a boost and buck-boost design topology.

3. THERMAL RESISTANCE

3.1 Basic Heat Transfer

The power dissipation in an IRED produces heat, which needs to be transferred to the ambient in order to prevent the junction temperature inside the IRED from reaching its maximum junction temperature. The second law of thermodynamics states that heat transfer occurs spontaneously from higher to lower temperature bodies, but never spontaneously in the reverse direction. The heat transfer path starts from the semiconductor junction layer into the ambient via the PCB and heatsink. This is shown in Fig. 13.

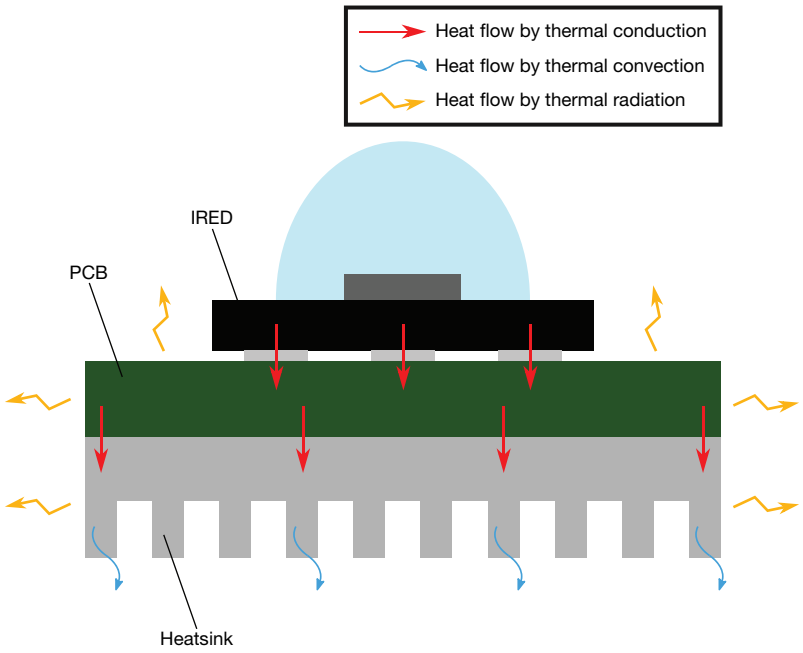

Fig. 13 - The Heat Flow From the IRED to the Ambient

Heat can travel from one place to another in three ways:

- Thermal conduction - heat transfer within the package, such as the connection pin, PCB, and heatsink
- Thermal convection - heat transfer from the surface of the package, PCB, and heatsink to the air / fluid
- Thermal radiation - heat transfer through the electromagnetic radiation by the heated surface of the package, PCB, and heatsink

3.2 Thermal Resistance Network

An electrical circuit analogy to model the series and parallel thermal resistance networks can be used for a heat flow analysis. When the thermal resistance of the respective circuit elements is known, the total series thermal resistance can therefore be computed as follows:

$$R_{th,\,series} = \sum_{n=1}^{i} R_{th,\,n} \quad (1)$$

Using the above analogy, a simple thermal resistance network consisting of only one IRED on a PCB and a heatsink can be modeled as shown below.

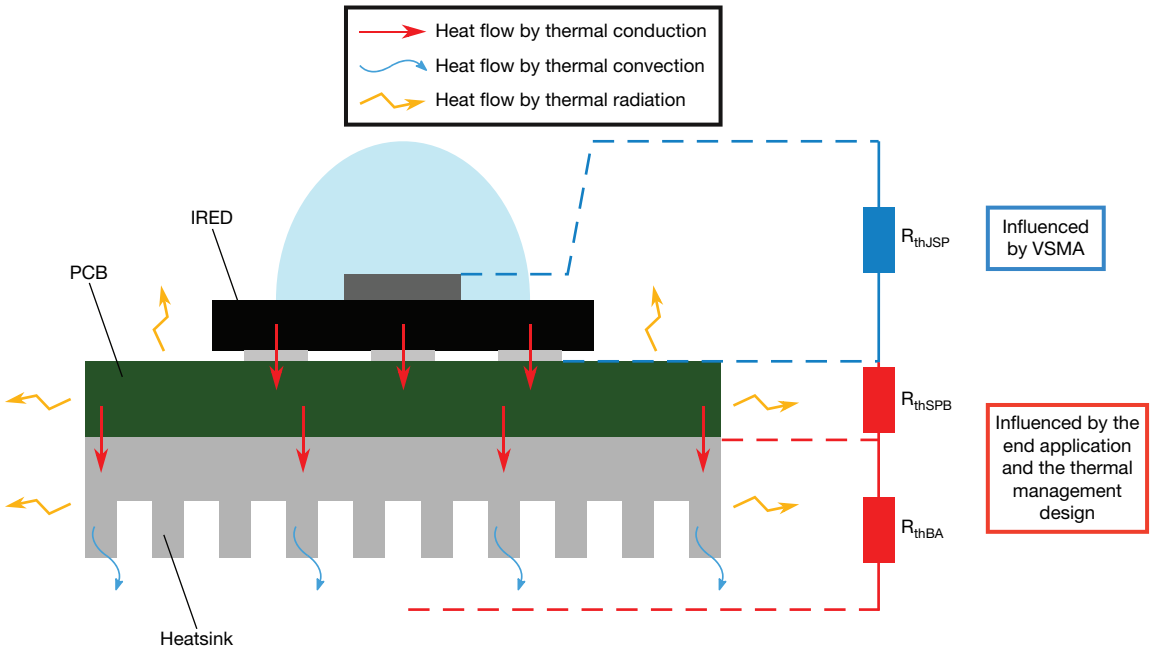

Fig. 14 - The Thermal Resistance Network Consists of an IRED, a PCB, and a Heatsink

The series thermal resistance network can be estimated to consist of the thermal resistance junction to solder point R_{thJSP}, the thermal resistance solder point to PCB R_{thSPB}, and the thermal resistance PCB to ambient R_{thBA}. Each thermal resistance includes the influence of thermal conduction, thermal convection, as well as thermal radiation, as described in the section Basic Heat Transfer. Therefore, the total thermal resistance in the system can be computed as follows:

$$R_{th,\,total} = R_{thJA} = R_{thJSP} + R_{thSPB} + R_{thBA} \tag{2}$$

where R_{thJA} is the thermal resistance junction to ambient. On the other hand, the total parallel thermal resistance can be computed as follows:

$$\frac{1}{R_{th,\,parallel}} = \sum_{n=1}^{i} \frac{1}{R_{th,\,n}} \tag{3}$$

If an array of IREDs is used on a PCB and a heatsink, both parallel and series thermal resistance networks can be used to model the thermal resistance, as shown in Fig. 15. The R_{thJSP} of the array will have a parallel connection and it will then be in series to R_{thSPB} and R_{thBA}. Therefore, the total thermal resistance in the system can be computed as follows:

$$R_{th,\,total} = R_{thJA} = \left(\frac{1}{R_{thJSP1}} + \frac{1}{R_{thJSP2}}\right)^{-1} + R_{thSPB} + R_{thBA} \tag{4}$$

Designing With the VSMA Series High Power IREDs

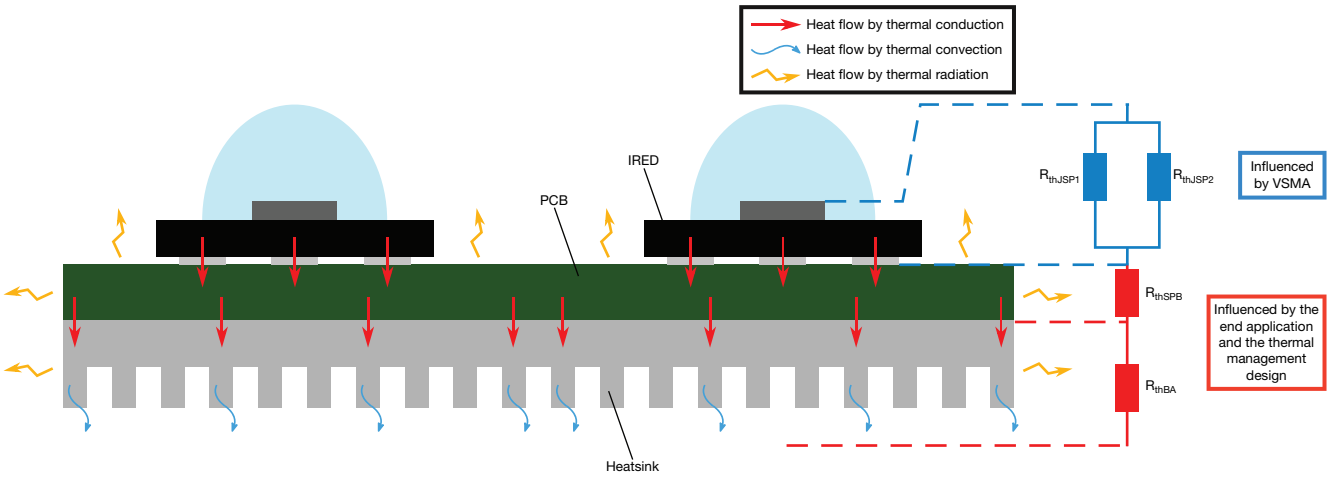

Fig. 15 - The Thermal Resistance Network of an Array of IREDs, a PCB, and a Heatsink

The packaging of the VSMA IRED has been designed with a low R_{thJSP} of typically 6 K/W. For the high power IRED market segment, it is an industry standard to state the thermal resistance in the datasheet only to the solder point. This allows a fair benchmark with the other available high power IREDs on the market. However, the actual thermal performance of an application depends on the thermal resistance junction to ambient R_{thJA}. This is influenced by the thermal management design of the PCB and the heatsink.

In practice, using either an insulated metal substrate (IMS) / metal core PCB or an FR4 PCB with thermal vias is recommended to operate at a higher driving current, which is commonly required for high power IRED applications. Table 4 shows the example of the thermal resistance stated in the absolute maximum ratings table in the datasheet of the VSMA series.

TABLE 4 - ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C, unless otherwise noted)

PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Thermal resistance junction to solder point real (1)	JESD 51	$R_{thJSP, real}$	5 to 9	K/W
Thermal resistance junction to ambient real	JESD 51	$R_{thJA, real}$	80	K/W

Note

(1) Thermal resistance junction to solder point real has been measured with the part mounted on an ideal heatsink and the optical output power has been deducted from the total electrical power dissipation

Here the terminologies $R_{thJA, real}$ and $R_{thJSP, real}$ have been used because in an IRED, only part of the supplied electrical power is converted to heat and the rest is converted to optical output power. This is neglected in the classical silicon-based semiconductors such as integrated circuits (IC), where it is assumed that all of the supplied electrical power is converted to heat.

Using this terminology, the thermal resistance electrical can be defined as follows:

$$R_{th, elec} = \frac{T_1 - T_2}{P_D} = \frac{T_1 - T_2}{P_{elec}} \quad (5)$$

APPLICATION NOTE

Designing With the VSMA Series High Power IREDs

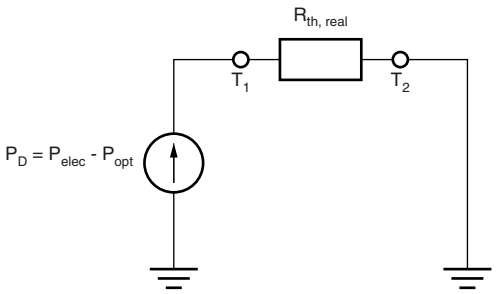

Fig. 16 - Thermal Resistance Real

The P_D term in Equation (5), which is converted to heat, can be adjusted to include the decoupled optical output into the equation, and the following thermal resistance real equation can be derived:

$$R_{th, real} = \frac{T_1 - T_2}{P_D} = \frac{T_1 - T_2}{P_{elec} - P_{opt}} \quad (6)$$

Fig. 16 shows the model of $R_{th, real}$. Using Equation (6), $Rt_{hJA, real}$ can be derived as follows:

$$R_{thJA, real} = \frac{T_j - T_{amb}}{P_D} = \frac{T_j - T_{amb}}{P_{elec} - P_{opt}} \quad (7)$$

Fig. 17 shows the thermal resistance network of the IRED in practice, where only $R_{thJA, real}$ will determine the thermal performance of the end application.

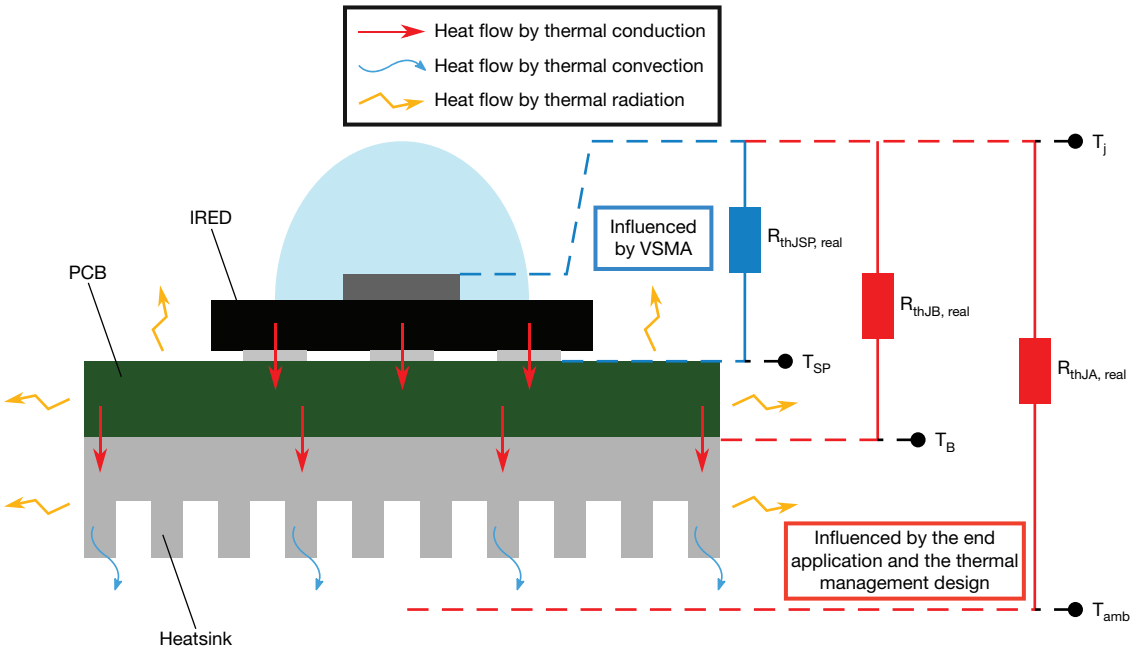

Fig. 17 - The Thermal Resistance Network of the IRED in Practice

APPLICATION NOTE

Using Equation (7), the junction temperature T_j can then be derived as follows:

$$T_j = ((P_{elec} - P_{opt}) \times R_{thJA,\,real}) + T_{amb} \tag{8}$$

Equation (8) can be modified as a function of the efficiency of the IRED η as follows:

$$T_j = ((P_{elec} \times (1 - \eta)) \times R_{thJA,\,real}) + T_{amb} \tag{9}$$

with η defined as follows:

$$\eta = \frac{P_{opt}}{P_{elec}} = \frac{\phi_e}{(V_F \times I_F)} \tag{10}$$

where ϕ_e is the radiant power at the defined V_F and I_F. These values can be found in the basic characteristics table of the IRED in the datasheets.

The above discussions of the thermal resistance network and junction temperature are only valid for DC operation. The dynamic continuous pulsed operation introduces the parasitic thermal capacitance effect apart from the thermal resistance real. This is shown by the thermal impedance equivalent circuit in Fig. 18.

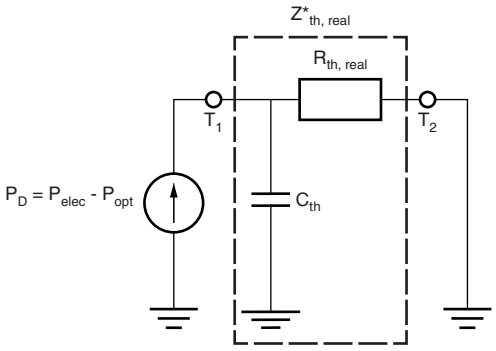

Fig. 18 - Thermal Impedance Real

The transient characteristics of the thermal impedance real $Z^*_{th,real}$ contain all the information about the thermal capacitance and thermal resistance contained in a heat path over time. Similar to $R_{th,real}$ in DC operation, $Z^*_{th,real}$ has considered the decoupled optical output power. The thermal impedance real $Z^*_{th,real}$ can therefore be derived as follows:

$$Z^*_{th,real} = \frac{T_1 - T_2}{P_D} = \frac{T_1 - T_2}{P_{elec} - P_{opt}} \tag{11}$$

The junction temperature T_j for the pulsed operation can then be derived as follows:

$$T_j = ((P_{elec} - P_{opt}) \times Z^*_{th,real}) + T_{amb} \tag{12}$$

$$= ((P_{elec} \text{ x } (1 - \eta)) \times Z^*_{th,real}) + T_{amb} \tag{13}$$

Example - Efficiency of IRED

With I_F = 1 A, $V_{F,\,typ.}$ = 2.9 V and $\phi_{e,\,typ.\,(1\,A)}$ = 1.450 W, η of the IRED is:

$$\eta = \frac{\phi_{e,\,typ.}}{(V_{F,\,typ.} \times I_F)} = \frac{1.450\ W}{(2.9\ V \times 1\ A)} = 0.5$$

APPLICATION NOTE

4. THERMAL MANAGEMENT DESIGN FOR DC OPERATION

Before starting the application development with the high power IRED, a solid understanding of the thermal resistance network should be gained, as discussed in Chapter 3. Fig. 17 shows the thermal resistance network of the IRED in practice, where the thermal resistance junction to ambient real $R_{thJA,\ real}$ will determine the thermal performance of the end application and not the thermal resistance junction to solder point real $R_{thJSP,\ real}$.

Besides that, the absolute maximum ratings need to be carefully adhered to. For DC operation, the highest forward current $I_{F,\ max.}$ will be 1.5 A. This is stated in the absolute maximum ratings table in the datasheet, as well as in Table 5. This is true for ambient temperature and $R_{thJA,\ real}$ up to certain limits. Therefore, the actual maximum allowable current depends on:

- PCB design - $R_{thJA,\ real}$
- T_{amb}

TABLE 5 - ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Reverse voltage		V_R	5	V
Minimum forward current		$I_{F,\ min.}$	100	mA
Forward current		I_F	1.5	A
Surge forward current	t_p = 100 µs	I_{FSM}	5	A
Power dissipation		P_V	5	W
Junction temperature		T_j	145	°C
Ambient temperature range		T_{amb}	-40 to +125	°C
Storage temperature range		T_{stg}	-40 to +125	°C
Soldering temperature	According to Fig. 11, J-STD020E	T_{sd}	260	°C
Thermal resistance junction to solder point real (1)	JESD 51	$R_{thJSP,real}$	5 to 9	K/W
Thermal resistance junction to ambient real	JESD 51	$R_{thJA,real}$	80	K/W
ESD sensitivity	According to ANSI / ESDA / JEDEC JS-001	V_{ESD}	5	kV

Notes

- Example of the absolute maximum ratings table for the VSMA1094250X02

(1) Thermal resistance junction to solder point real has been measured with the part mounted on an ideal heatsink and the optical output power has been deducted from the total electrical power dissipation

A low $R_{thJA,\ real}$ is desired to ensure optimum heat flow from the IRED to the surroundings, limiting the total temperature increase in the system. This prevents T_j from exceeding the specified maximum junction temperature of 145 °C in the absolute maximum ratings table.

A low $R_{thJA,\ real}$ can be achieved via a thought-out thermal management design by implementing the following:

- Select PCB technology that has a high thermal conductivity, such as metal core / insulated metal substrate (IMS) PCB
- Incorporate a heatsink into the thermal management design
- Proper solder connection of the middle anode pin
- Incorporate thermal design elements such as
  - Thermal vias
  - Enlarged solder pads
  - Thicker copper layers

  to improve heat distribution, especially when typical FR4 PCB technology is used

Equation (8) defines the junction temperature. Any change in

- IRED operating point I_F and V_F (hence, both P_{elec} and P_{opt} are affected as well)
- $R_{thJA,\ real}$ (thermal management design)
- T_{amb}

will affect T_j. Therefore, these parameters must be carefully selected when designing the end application to ensure that T_j never exceeds the limit of 145 °C.

4.1 DC Derating Diagram

A DC derating diagram is a starting point when designing with high power IREDs for DC operation. This diagram indicates the maximum allowable driving current as a function of ambient temperature. Fig. 19 shows the general DC derating diagram of the VSMA series. The maximum allowable current for DC operation is 1.5 A. The maximum junction temperature for the VSMA series is 145 °C and the operation of the IRED in the ambient temperature is limited to 125 °C. In general, the maximum allowable current increases with decreasing $R_{thJA, real}$. Therefore, if high DC current operation is required for the application, PCB technology with low $R_{thJA, real}$, such as metal core / IMS, is a good starting point.

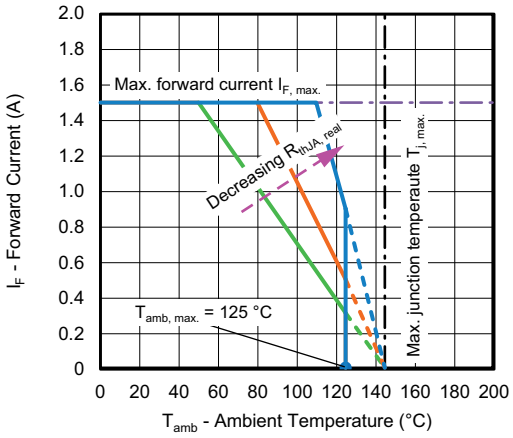

Fig. 19 - General DC Derating Diagram

There are four important points needed to build the derating diagram, as shown in Fig. 20:

- Point 1:
  Starting point of $I_{F, max.}$ = 1.5 A DC limit (Point 1 can also be located at T_{amb} < 0 °C for higher $R_{thJA, real}$, as shown in Fig. 20)
- Point 2:
  $T_{amb, max.}$ for the given $R_{thJA, real}$, so that the part can be driven up to the rated 1.5 A and T_j never exceeds 145 °C

$$T_{amb, max.} = T_{j, max.} - (((V_F \times I_{F, max.}) - P_{opt}) \times R_{thJA, real}) = T_{j, max.} - ((V_F \times I_{F, max.} \times (1 - \eta)) \times R_{thJA, real}) \quad (14)$$

  Note
  - $V_F = V_{F, max.}$ is typically used to account for part to part tolerance
- Point 3:
  $I_{F, max.}$ at $T_{amb, max.}$ = 125 °C for the given $R_{thJA, real}$

$$I_{F, max.} = \frac{\frac{T_{j, max.} - T_{amb, max.}}{R_{thJA, real}} + P_{opt}}{V_F} = \frac{T_{j, max.} - T_{amb, max.}}{(R_{thJA, real} \times V_F) \times (1 - \eta)} \quad (15)$$

- Point 4:
  $T_{amb, max.}$ = 125 °C due to maximum rated limit

APPLICATION NOTE

Designing With the VSMA Series High Power IREDs

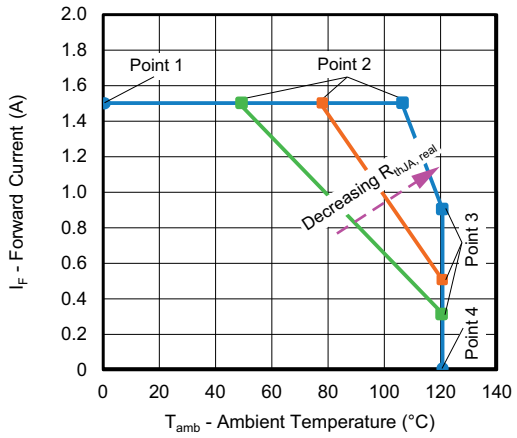

Fig. 20 - Four Important Points on DC Derating Diagram

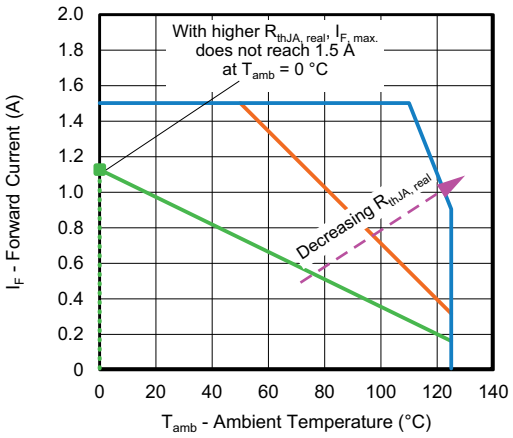

Fig. 21 - The Effect of Higher $R_{thJA, real}$

The given DC derating diagram in the datasheet is based on the thermal resistance junction to solder point R_{thJSP}. This is shown in Fig. 22. This derating diagram is useful when comparing with other parts for benchmarking purposes. The overall thermal resistance depends on the thermal management design in the end application, as shown in Fig. 17.

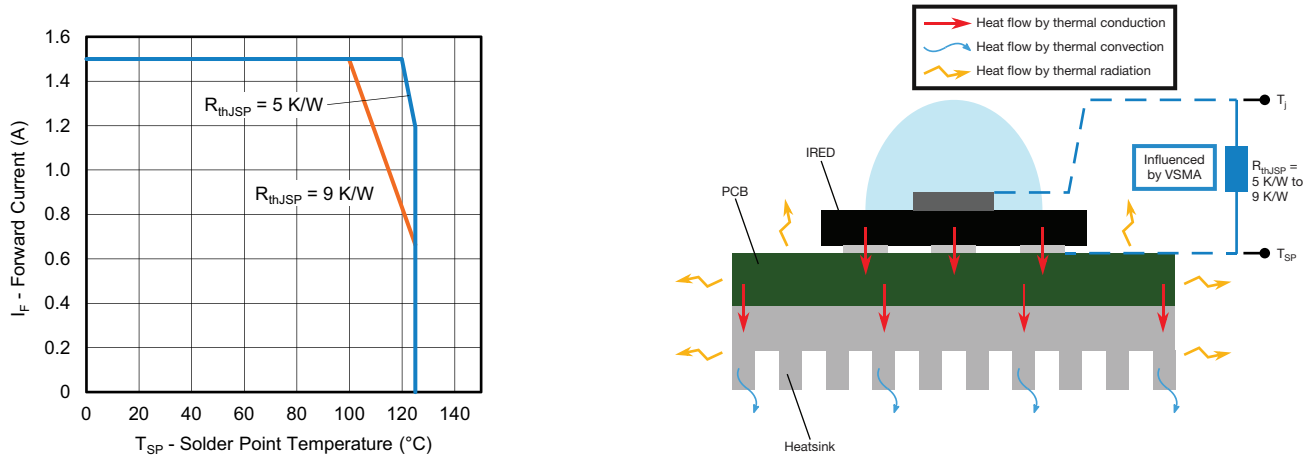

Fig. 22 - Derating Diagram Based on R_{thJSP}, Which is Given in the Datasheet

APPLICATION NOTE

Designing With the VSMA Series High Power IREDs

The derating diagram based on $R_{thJA, real}$ can be used as a design reference when designing with the IRED, as the overall thermal influence of the system will play a role in the increase of temperature. Several derating curves are given in Fig. 23 based on typical $R_{thJA, real}$ from typical PCB technologies, as well as available thermal design elements. It can be observed that the maximum allowable current increases with decreasing $R_{thJA, real}$.

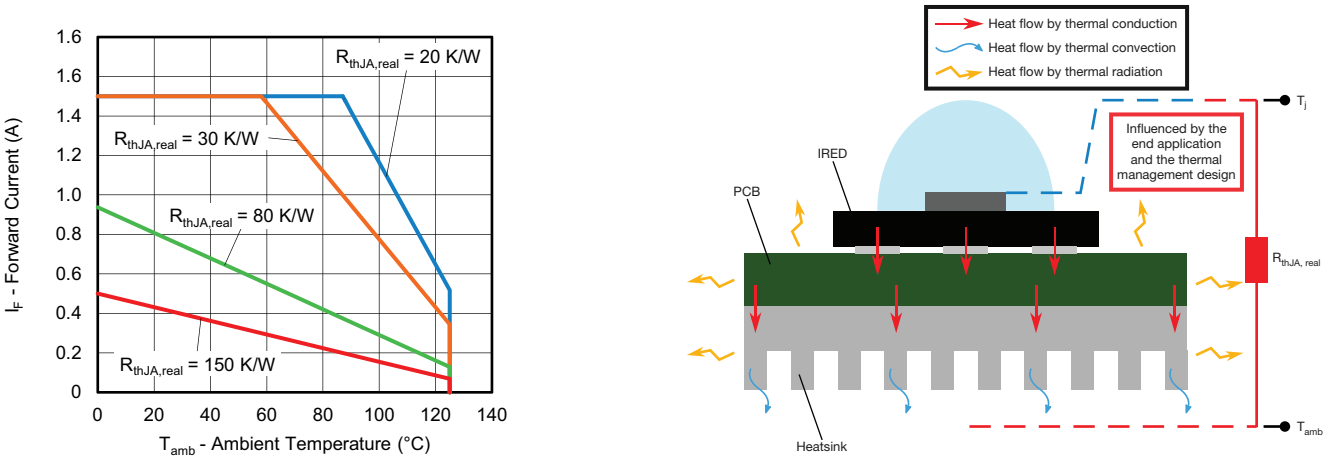

Fig. 23 - Derating Diagram Based on $R_{thJA, real}$, Which is Useful for Design Reference

Examples of $R_{thJA, real}$ values from typical PCB technologies, as well as available thermal design elements, are shown below.

TABLE 6 - THERMAL RESISTANCE JUNCTION TO AMBIENT REAL $R_{thJA, real}$ FOR DIFFERENT PCB TECHNOLOGIES

PCB TECHNOLOGY	SYMBOL	VALUE	UNIT
Metal core / insulated metal substrate (IMS) PCB with heatsink	$R_{thJA, real}$	20	K/W
Metal core / insulated metal substrate (IMS) PCB without heatsink		30	
FR4 PCB with thermal vias		80	
Standard FR4 PCB		150	

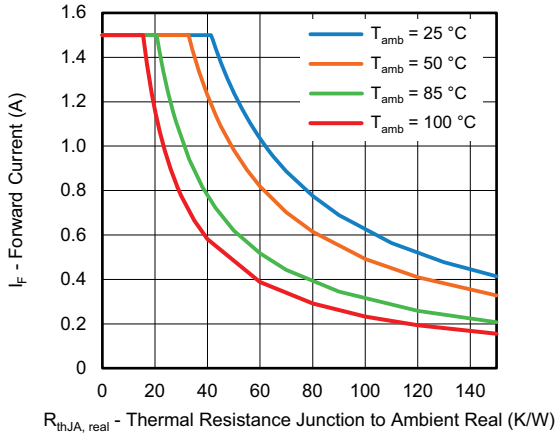

Fig. 24 - Forward Current vs. Thermal Resistance Junction to Ambient Real

APPLICATION NOTE

Designing With the VSMA Series High Power IREDs

The forward current in Fig. 23 can also be plotted against $R_{thJA, real}$, as shown in Fig. 24. This way, the designer can quickly find the minimum required $R_{thJA, real}$ for several operating ambient temperatures. An important design parameter extracted in this diagram is the $R_{thJA, real}$ required to fulfill the minimum radiant intensity requirement at the high limit ambient temperature. In many applications, this temperature limit is 85 °C.

For the VSMA series, the middle anode connection also improves the heat flow and reduces the thermal resistance. Consequently, the increase in temperature reduces as well. A proper solder connection of this middle anode pin is imperative to improving the heat flow. Otherwise, the rise of $R_{thJA, real}$ up to 3 K/W, in addition to the stated values in Table 6, can be expected. Please note that the $R_{thJA, real}$ values in Table 6 above are based on the typical best case and optimized design scenario. The actual $R_{thJA, real}$ may vary depending on the end application and other external factors. Besides, the derating diagram in Fig. 23 does not consider the temperature effect on V_F and radiant power ϕ_e.

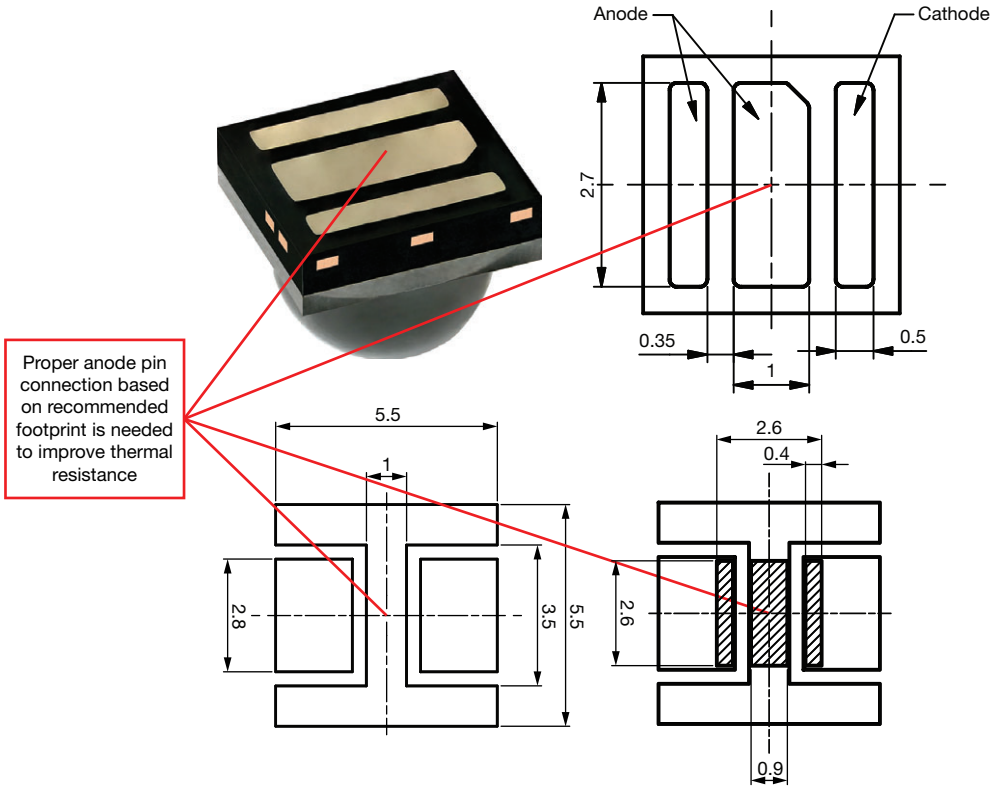

Fig. 25 - Anode Pin Connection in the Middle of the VSMA1094250X02

APPLICATION NOTE

4.2 Using the Given DC Derating Diagram

The DC derating diagram in Fig. 23 should cover the frequently used PCB technologies. These can be used to estimate the $R_{thJA,\ real}$ if system-level measurements are unavailable, and help to determine the operating point limits of I_F and T_{amb} during the design phase. This approach would enable the designer to identify and estimate the maximum allowable operating point to prevent the IRED from getting damaged.

The safer approach when using this method is to leave a buffer or safety margin from the typical known $R_{thJA,\ real}$ of the selected PCB technology. For example, when using a metal core / IMS PCB without a heatsink with a typical $R_{thJA,\ real}$ = 30 K/W, it is common to leave a safety margin when selecting the operating point I_F and T_{amb}, as shown in Fig. 26 below, to accommodate for possible fluctuations in the ambient conditions.

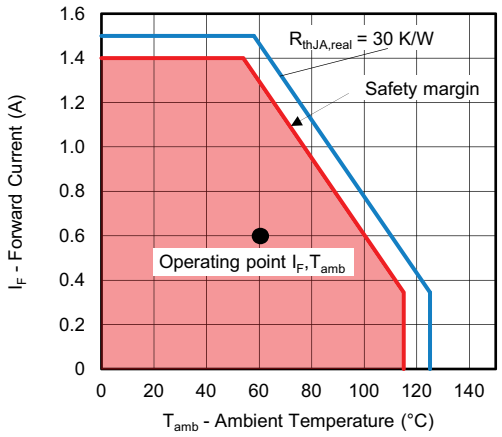

Fig. 26 - Derating Diagram With Safety Margin

A suitable safety margin can be defined depending on the design requirements. This ensures that $T_{j,\ max.}$ = 145 °C will not be exceeded, especially when the exact $R_{thJA,\ real}$ is not known. A safety margin also helps reduce the degradation and helps prolong the lifetime of the IRED. Any selection of the operating point I_F and T_{amb} within the red zone in Fig. 26 above would ensure that T_j does not reach $T_{j,\ max.}$ = 145 °C.

APPLICATION NOTE

Designing With the VSMA Series High Power IREDs

4.3 Real-World Design Examples

In this section, some real-world examples will be discussed to guide the designer on possible design approaches. The design parameters of an IRED, such as $R_{thJA, real}$, I_e, ϕ_e, and V_F, change with temperature. Therefore, the examples below will guide the designer on the possible design approaches with the VSMA series, given any limits on design parameters that are affected by the thermal effect.

The examples use the basic characteristics of the VSMA1094250X02.

TABLE 7 - BASIC CHARACTERISTICS FOR THE VSMA1094250X02
(T_{amb} = 25 °C, unless otherwise noted)

PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Forward voltage	I_F = 0.35 A, t_p = 10 ms	V_F	2.1	2.7	3.0	V
	I_F = 1 A, t_p = 100 µs	V_F	2.2	2.9	3.1	V
	I_F = 1.5 A, t_p = 100 µs	V_F	2.6	3.1	3.35	V
	I_F = 5 A, t_p = 100 µs	V_F	2.7	3.8	4.2	V
Radiant intensity (1)	I_F = 0.35 A, t_p = 10 ms	I_e	415	500	670	mW/sr
	I_F = 1 A, t_p = 100 µs	I_e	1120	1350	1800	mW/sr
	I_F = 1.5 A, t_p = 100 µs	I_e	1660	2000	2700	mW/sr
	I_F = 5 A, t_p = 100 µs	I_e	4975	6000	8000	mW/sr
Radiant power	I_F = 1 A, t_p = 100 µs	ϕ_e	-	1450	-	mW
	I_F = 1.5 A, t_p = 100 µs	ϕ_e	-	2125	-	mW
Temperature coefficient of ϕ	I_F = 1 A, t_p = 100 µs	TK_ϕ	-	-0.15	-	%/K

Note

(1) The radiant intensity values have been measured with a tolerance of ± 11 %

Example - Known Thermal Resistance

When designing an application, the designer is often limited to a specific PCB technology. For example, if the $R_{thJA, real}$ of the PCB is known, a DC derating diagram can be constructed for the designer to derive the maximum allowed driving current, its corresponding radiant intensity, and the maximum permitted operating ambient temperature. The DC derating diagram can be constructed by calculating the four points indicated in Fig. 20, as well as using the Equations (10), (14), and (15).

Given the $R_{thJA, real}$ design requirement of 40 K/W, the DC derating diagram can be constructed by calculating the two points below, apart from point 1, which is limited at 1.5 A, and point 4, which is limited at 125 °C.

- Calculate point 2 from Equation (14)

$$T_{amb, max.} = T_{j, max.} - (((V_F \times I_{F, max.}) - P_{opt}) \times R_{thJA, real})$$
$$= 145\ °C - (((3.35\ V \times 1.5\ A) - 2.125\ W) \times 40\ °C/W) = 29\ °C$$

Note

- $V_{F, max.}$ = 3.35 V has been used instead of $V_{F, typ.}$ = 3.1 V to consider the worst case scenario. $P_{opt} = \phi_{e, typ.}$

- Calculate point 3 from Equation (10) and (15)

$$I_{F, max.} = \frac{\frac{T_{j, max.} - T_{amb, max.}}{R_{thJA, real}} + P_{opt}}{V_F} = \frac{T_{j, max.} - T_{amb, max.}}{(R_{thJA, real} \times V_F) \times (1 - \eta)} = \frac{145\ °C - 125\ °C}{(40\ °C/W \times 3.35\ V) \times (1 - 0.423)} = 0.259\ A$$

Note

- $V_{F, max.}$ = 3.35 V at $I_{F, max.}$ = 1.5 A has been used instead of $V_{F, max.}$ at the exact $I_{F, max.}$ at point 3 to account for part to part tolerance. This also reduces the complexity of the calculation because both points relate to each other in power function behavior. η is the efficiency of the IRED at 1.5 A, which is defined as

$$\eta = \frac{\phi_{e, typ.}}{(V_{F, max.} \times I_{F, max.})} = \frac{2.125\ W}{(3.35\ V \times 1.5\ A)} = 0.423$$

Fig. 27 shows the DC derating diagram for the PCB requirement of $R_{thJA, real}$ = 40 K/W. The corresponding radiant intensity of the maximum permitted forward current for each point on the DC derating diagram can be derived from the relative radiant intensity vs. forward current in the datasheet.

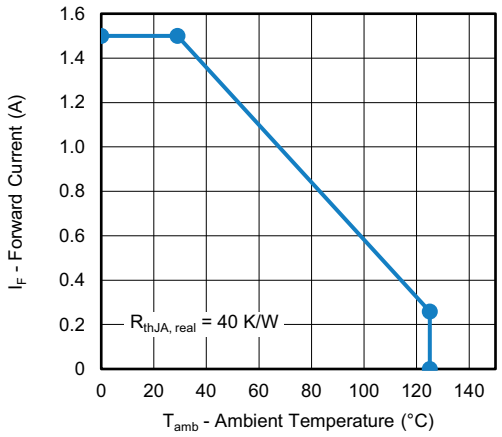

Fig. 27 - DC Derating Diagram With $R_{thJA, real}$ = 40 K/W

Example - Given Radiant Power Budget

The radiant power of an IRED decreases with increasing temperature. Therefore, it is recommended to design a system with a radiant power buffer, given the ambient temperature fluctuation. Some applications, such as CCTV illumination and driver monitoring, have a specified radiant power budget to fulfill the minimum SNR requirement of the camera. If, for example, the camera needs to accommodate a radiant power loss of 15 % and minimum radiant intensity of 974 mW/sr, the designer can then design the thermal management to fulfill this requirement. The operating point I_F has to be selected so that the radiant intensity is 115 % higher at a typical operating temperature, such as 25 °C. The following steps describe the calculation needed to find the highest allowable $R_{thJA, real}$ to stay within the radiant power budget limitation above:

- Step 1:
  Calculate the radiant intensity required at a typical operating temperature and the corresponding I_F to fulfill the minimum radiant intensity requirement of 974 mW/sr, given a radiant power budget of 15 %

$$I_{e, min. (25\ °C)} = \frac{100\ \% + \text{power budget}}{100\ \%} \times I_{e, min.} = \frac{100\ \% + 15\ \%}{100\ \%} \times 974\ \text{mW/sr} = \frac{115\ \%}{100\ \%} \times 974\ \text{mW/sr} \approx 1120\ \text{mW/sr} \quad (16)$$

- Step 2:
  Find the corresponding I_F towards the $I_{e, min. (25\ °C)}$. From Table 7, an I_F of 1 A provides $I_{e, min. (25\ °C)}$ of 1120 mW/sr
- Step 3:
  Calculate the increase of temperature due to the radiant power loss from the temperature coefficient of radiant power TK_ϕ stated in the basic characteristics table in Table 7 or in the datasheet

$$\Delta T = T_j - T_{amb} = \frac{\Delta\phi_{e, loss}}{TK_\phi} = \frac{15\ \%}{0.15\ \%/°C} = 100\ °C \quad (17)$$

- Step 4:
  Calculate the maximum allowable $R_{thJA, real}$ using Equation (7)

$$R_{thJA, real} = \frac{T_j - T_{amb}}{P_{elec} - P_{opt}} = \frac{100\ °C}{(3.1\ V \times 1\ A) - 1.45\ W} = \frac{100\ °C}{3.1\ W - 1.45\ W} = 60.61\ K/W$$

Note

- From Table 7, P_{opt} at I_F = 1 A and $I_{e, min. (25\ °C)}$ = 1120 mW/sr is 1.45 W. $V_{F, max.}$ = 3.1 V at I_F = 1 A has been used instead of $V_{F, typ.}$ for the P_{elec} calculation to account for part to part tolerance

Example - Given Optical Requirement

In a real-world application, the minimum radiant intensity required by a system is typically given. If, for example, the required $I_{e, min.}$ is 1120 mW/sr, the corresponding I_F according to the datasheet is 1 A. Besides that, the designer could also be limited to a PCB with a fixed $R_{thJA, real}$. Considering these design requirements, the designer can extract the $T_{amb, max.}$, given a fixed $R_{thJA, real}$, from the DC derating diagram, as shown in Fig. 28, or from the calculation using Equation (14).

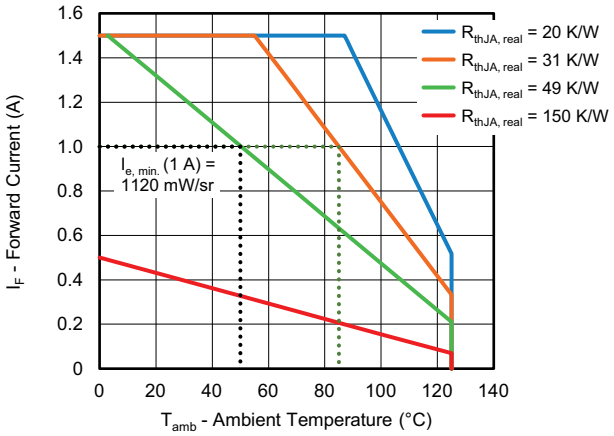

Fig. 28 - Derating Diagram Based on $R_{thJA, real}$

In the case of $I_{e, min.}$ = 1120 mW/sr given a metal core PCB with $R_{thJA, real}$ = 31 K/W, the allowed $T_{amb, max.}$ according to the DC derating diagram and Equation (14) is 85 °C.

$$T_{amb, max.} = T_j - (((V_F \times I_{F, max.}) - P_{opt}) \times R_{thJA, real}) = T_j - (((V_F \times I_{F, max.}) \times (1 - \eta)) \times R_{thJA, real})$$
$$= 145\ °C - (((3.35\ V \times 1\ A) \times (1 - 0.423)) \times 31\ °C/W) = 85\ °C$$

The application can only operate until $T_{amb, max.}$ = 85 °C given the design limitation. This is indicated by the green dotted line in Fig. 28. Otherwise, the maximum junction temperature will be exceeded. If a higher operating ambient temperature is required, an improvement in the thermal management design or a reduced I_F is required. On the other hand, if the optical design requirement is $I_{e, min.}$ = 1120 mW/sr and a PCB with $R_{thJA, real}$ = 49 K/W is given, the allowed $T_{amb, max.}$ is 50 °C, as shown by the black dotted line in Fig. 28.

Apart from the above situation, the designer could have a design limitation of a fixed $T_{amb, max.}$ requirement in the system, but with the flexibility in thermal management design for the PCB. Therefore, the required $R_{thJA, real}$ for the PCB can also be extracted from the I_F vs. $R_{thJA, real}$ diagram, as shown in Fig. 29, or from the calculation using Equation (7).

Designing With the VSMA Series High Power IREDs

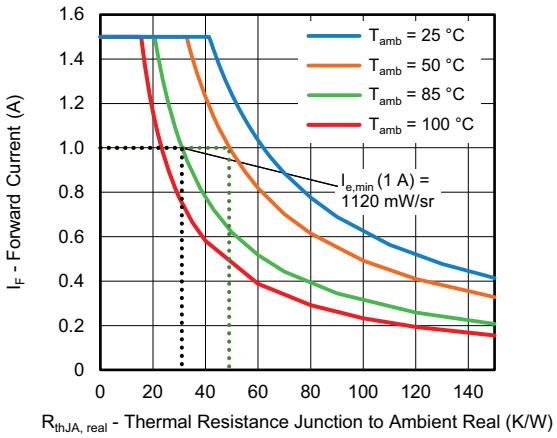

Fig. 29 - Forward Current vs. Thermal Resistance Junction to Ambient Real

A typical $T_{amb, max.}$ in many applications is 85 °C. Given a similar $I_{e, min.}$ = 1120 mW/sr, with an I_F = 1 A requirement for the application as mentioned before, the required $R_{thJA, real}$ according to the I_F vs. $R_{thJA, real}$ diagram and Equation (7) is 31 K/W.

$$R_{thJA, real} = \frac{T_j - T_{amb}}{P_{elec} - P_{opt}} = \frac{T_j - T_{amb}}{(P_{elec}) \times (1 - \eta)} = \frac{145\ °C - 85\ °C}{(3.35\ V \times 1\ A) \times (1 - 0.423)} = 31\ K/W$$

The designer has to design a metal core PCB with $R_{thJA, real}$ = 31 K/W to prevent the maximum junction temperature from being exceeded. This is indicated by the black dotted line in Fig. 29. In the case of $I_{e, min.}$ = 1120 mW/sr and $T_{amb, max.}$ = 50 °C, the required $R_{thJA, real}$ of the PCB is 49 K/W. This is indicated by the green dotted line in Fig. 29.

5. THERMAL MANAGEMENT DESIGN FOR PULSED OPERATION

A basic understanding of the thermal resistance network and the thermal impedance discussed in Chapter 3 is required for the application's development using a high power IRED with pulsed operation. Fig. 17 shows the thermal resistance network of the IRED, where the total thermal resistance in the system equals the thermal resistance junction to ambient real $R_{thJA,\ real}$ and will determine the thermal performance of the end application.

The actual maximum allowable pulsed current depends on:

- PCB design - $Rt_{hJA,\ real}$
- T_{amb}
- Pulse duration t_p
- Duty cycle D

Compared to DC operation, the designer has two additional interrelated parameters when designing the IRED for the end application - pulse duration and duty cycle. Information on both can be found in the pulse derating diagram. The absolute maximum ratings table shows that the IRED could be driven with pulsed operation up to 5 A. However, driving the IRED with a lower pulsed forward current is recommended to extend the lifetime.

TABLE 8 - ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Reverse voltage		V_R	5	V
Minimum forward current		$I_{F,\ min.}$	100	mA
Forward current		I_F	1.5	A
Surge forward current	t_p = 100 µs	I_{FSM}	5	A
Power dissipation		P_V	5	W
Junction temperature		T_j	145	°C
Ambient temperature range		T_{amb}	-40 to +125	°C
Storage temperature range		T_{stg}	-40 to +125	°C
Soldering temperature	According to Fig. 11, J-STD020E	T_{sd}	260	°C
Thermal resistance junction to solder point real (1)	JESD 51	$R_{thJSP,real}$	5 to 9	K/W
Thermal resistance junction to ambient real	JESD 51	$R_{thJA,real}$	80	K/W
ESD sensitivity	According to ANSI / ESDA / JEDEC JS-001	V_{ESD}	5	kV

Note

(1) Thermal resistance junction to solder point real has been measured with the part mounted on an ideal heatsink and the optical output power has been deducted from the total electrical power dissipation.

APPLICATION NOTE

5.1 Pulse Derating Diagram

A pulse derating diagram indicates the maximum allowable driving current as a function of t_p, D, T_{amb}, and $R_{thJA, real}$ before the specified maximum junction temperature is exceeded. Fig. 30 shows the general pulse derating diagram of the VSMA series. The maximum allowable current for the best-case scenario in pulsed operation is 5 A. This is indicated by the surge forward current I_{FSM} in the absolute maximum ratings table in the datasheet. The decreasing transient behavior of the maximum allowable current with pulse duration is due to the system's thermal impedance introduced by the pulse's parasitic thermal capacitance effect. The maximum allowable pulsed current increases with decreasing duty cycle D for the same $R_{thJA, real}$ and T_{amb}. On the other hand, the pulse derating diagram differs for every $R_{thJA, real}$ and T_{amb}. In this application note, only diagrams at 25 °C and 85 °C for metal core and FR4 PCB will be provided to indicate the typical and maximum operating ambient temperature. These diagrams can be used to estimate the pulse derating diagram at different $R_{thJA, real}$ and T_{amb}.

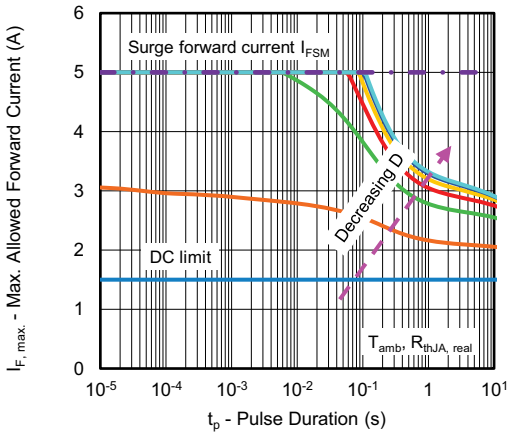

Fig. 30 - General Pulse Derating Diagram

The maximum allowable pulsed current increases with decreasing $R_{thJA, real}$ and T_{amb}. If a high pulsed current operation is required for the application, PCB technology with low $R_{thJA, real}$, such as metal core / IMS, and operation at room temperature will be a good starting point.

The datasheet provides the pulse derating diagram based on the thermal resistance junction to solder point R_{thJSP} standard, as shown in Fig. 31. This derating diagram is helpful for part benchmarking purposes, as it considers thermal heat transfer until the solder point. This is usually influenced by the manufacturer's thermal package design. Therefore, it does not convey a real-life scenario like the $R_{thJA, real}$, where it takes into account the thermal management design of the end application, as shown in Fig. 17.

Designing With the VSMA Series High Power IREDs

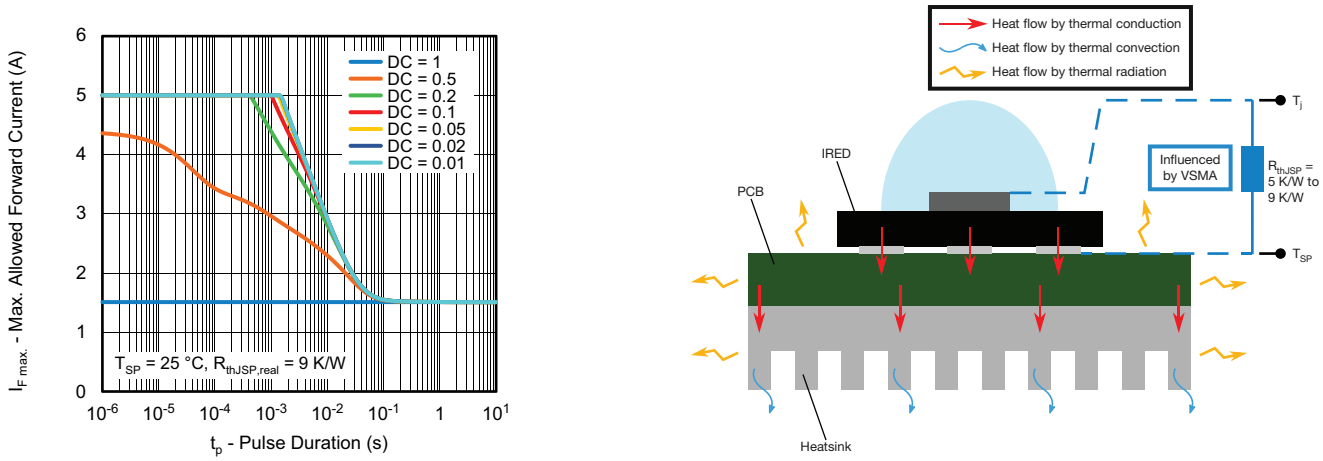

Fig. 31 - Pulse Derating Diagram Based on R_{thJSP}, Which is Given in the Datasheet

Fig. 33 shows an example of the pulse derating diagram based on the measurement of the required thermal parameters and calculation of the thermal impedance equivalent circuit in Fig. 18. As discussed in Section 3.2, the dynamic continuous pulsed operation introduces the parasitic thermal capacitance effect. This means the thermal impedance junction to ambient real $Z^*_{thJA,\,real}$ increases with pulse duration until it reaches a steady state, as shown in Fig. 32. The $Z^*_{thJA,\,real}$ value is a transient quantity containing all the information about the thermal capacitance and resistance contained in a heat path over time. Thus, $Z^*_{thJA,\,real}$ is used as a basis for calculating the pulse derating diagram. In contrast, the $R_{thJA,\,real}$ is a scalar quantity in each operating point in the pulse derating diagram. Therefore, $R_{thJA,\,real}$ is the terminology used to describe the system's thermal resistance at an operating point. Besides that, one can compare Fig. 32 and Fig. 33 on the effect of the $Z^*_{thJA,\,real}$ and maximum allowed forward current at both shorter and longer pulse durations for all duty cycles.

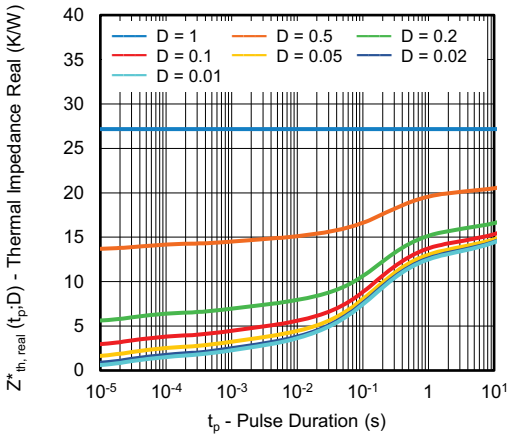

Fig. 32 - $Z^*_{th,\,real}$ vs. Pulse Duration

APPLICATION NOTE

Designing With the VSMA Series High Power IREDs

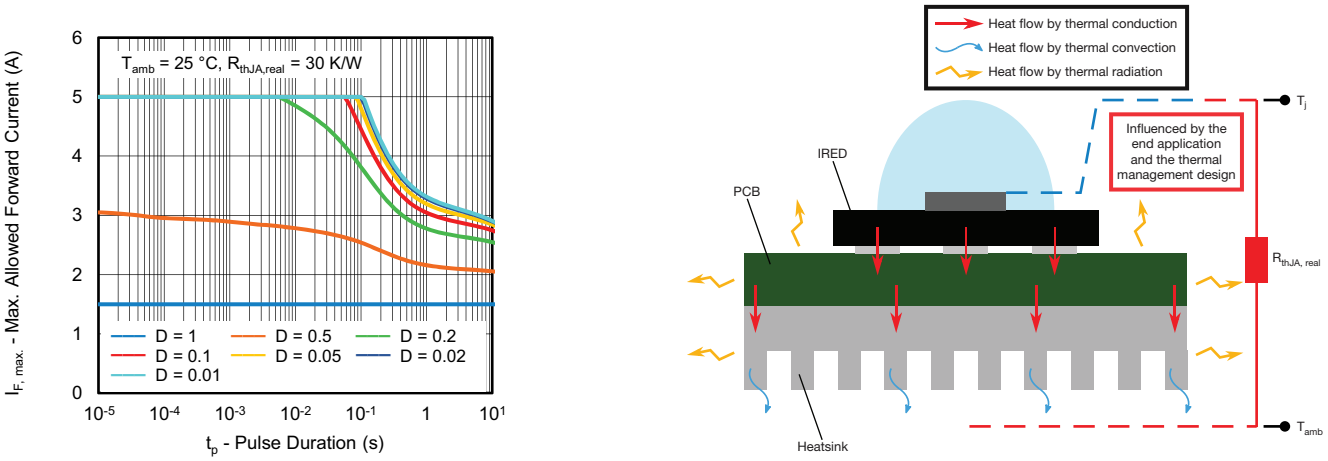

Fig. 33 - Pulse Derating Diagram Based on R_{thJA}, Which is Useful for Design Reference

Since the total thermal resistance of the system will play a role in the increase in temperature, the use of the pulse derating diagram based on $R_{thJA,\ real}$ for a design reference is a must when designing with an IRED. Several derating curves are given in the next page based on the $R_{thJA,\ real}$ from the typical PCB technologies, as well as available thermal design elements. Examples of $R_{thJA,\ real}$ values from typical PCB technologies, as well as available thermal design elements, are shown below.

TABLE 9 - THERMAL RESISTANCE JUNCTION TO AMBIENT REAL $R_{thJA,\ real}$ FOR DIFFERENT PCB TECHNOLOGIES

PCB TECHNOLOGY	SYMBOL	VALUE	UNIT
Metal core / insulated metal substrate (IMS) PCB with heatsink	$R_{thJA,\ real}$	20	K/W
Metal core / insulated metal substrate (IMS) PCB without heatsink		30	
FR4 PCB with thermal vias		80	
Standard FR4 PCB		150	

The $R_{thJA,\ real}$ values in Table 9 are based on the typical best case and optimized design scenario. A proper solder connection in the middle anode pin described in Section 4.1 improves the heat flow. The lack of a proper solder connection of this pin increases the $R_{thJA,\ real}$ value up to 3 K/W, in addition to the stated values in Table 9. After all, the actual $R_{thJA,\ real}$ may vary depending on the end application and other external factors.

Designing With the VSMA Series High Power IREDs

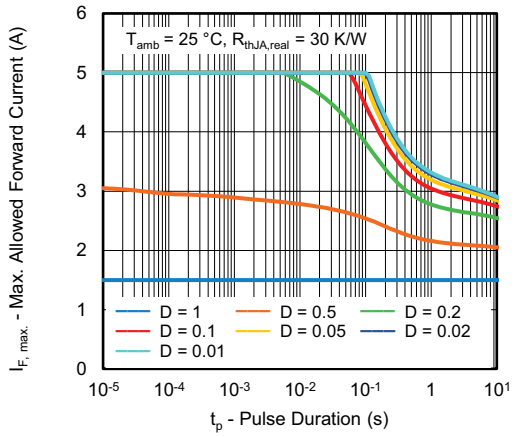

Fig. 34 - Pulse Derating Diagram Based on Metal Core PCB at 25 °C

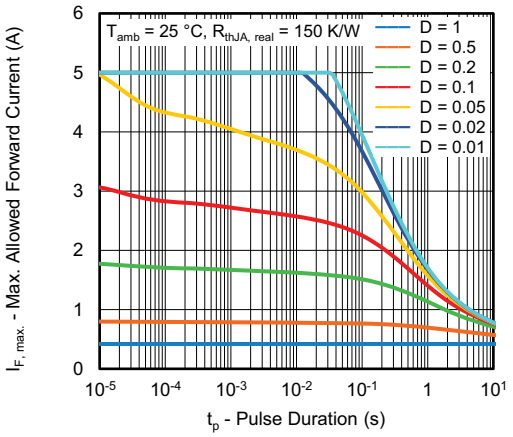

Fig. 35 - Pulse Derating Diagram Based on FR4 PCB at 25 °C

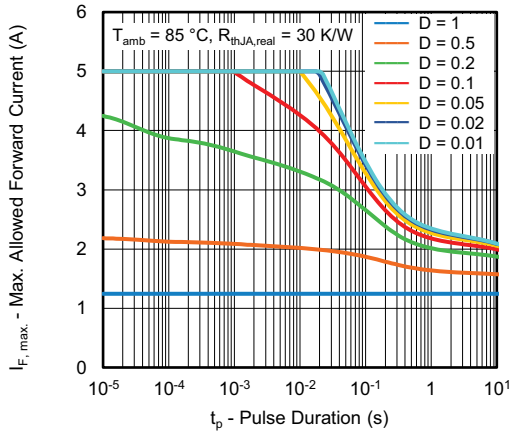

Fig. 36 - Pulse Derating Diagram Based on Metal Core PCB at 85 °C

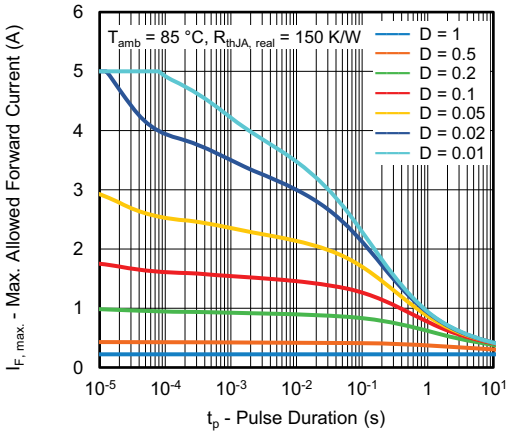

Fig. 37 - Pulse Derating Diagram Based on FR4 PCB at 85 °C

5.2 Using the Pulse Derating Diagram

As described in Section 2.3, another approach to operating the IRED is by periodically or intermittently pulsing the IRED on and off. This approach is known as PWM, where the IRED is driven by varying the driving current I_F with a pulse duration of t_p and is repeated with a period of T. The pulse will then have a duty cycle D of t_p/T. This is shown in Fig. 38.

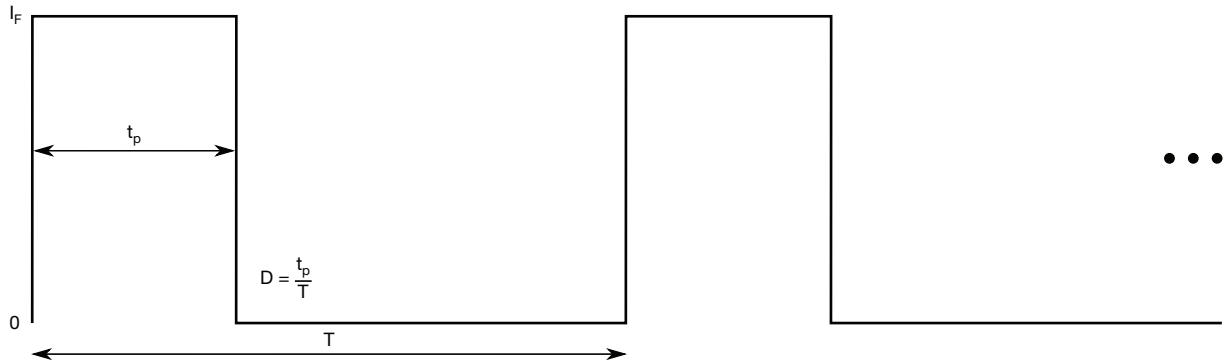

Fig. 38 - Pulsed Operation Example

The parameters I_F, t_p, or D based on the pulse derating diagram in Fig. 34, Fig. 35, Fig. 36, and Fig. 37 can be adjusted to change the intensity of the IRED. The given four-pulse derating diagrams cover the frequently used PCB technologies. This helps estimate the $R_{thJA, real}$ and T_{amb} to find the operating point I_F, t_p, or D during the design phase.

Example - How to Read Maximum Allowable Forward Current

If an application requires a metal core PCB with $R_{thJA, real}$ = 30 K/W, an operation at T_{amb} = 25 °C, a duty cycle of D = 0.2, and a pulse duration of t_p = 10 ms, the maximum allowable forward current is 4.85 A. This is shown in Fig. 39.

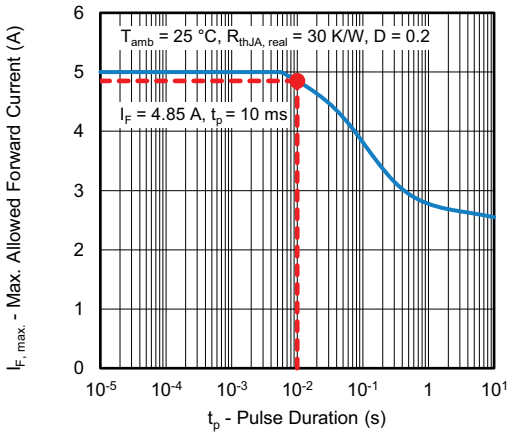

Fig. 39 - Reading the Maximum Allowable Forward Current or Pulse Duration on the Pulse Derating Diagram

The reverse is also true when the designer is limited with $R_{thJA, real}$ = 30 K/W, an operation at T_{amb} = 25 °C, a duty cycle of D = 0.2, and maximum allowable forward current of I_F = 4.85 A. The maximum allowable pulse duration is t_p = 10 ms.

Pulse Derating Diagram With Safety Margin

It is safer to provide a buffer or safety margin when reading the pulse derating diagram of the selected $R_{thJA, real}$. For example, when a metal core PCB without a heatsink with a typical $R_{thJA, real}$ = 30 K/W has been chosen, it is safer to create a safety margin when selecting the operating point I_F, t_p, and D, as shown in Fig. 40 below.

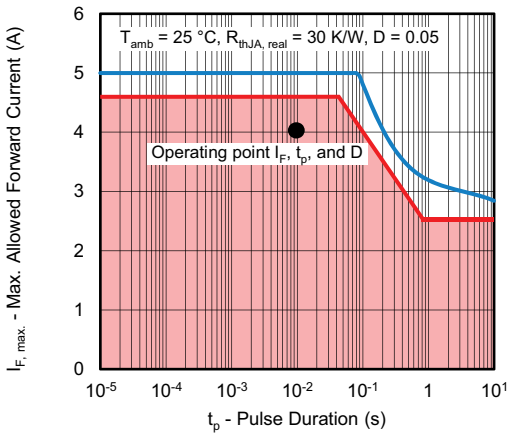

Fig. 40 - Pulse Derating Diagram With Safety Margin

As discussed in Section 4.2, a suitable safety margin prevents the maximum junction temperature from being exceeded, especially when the exact $R_{thJA, real}$ is not known.

6. CONCLUSION

Designing an application with a high power IRED requires knowledge of the electrical properties of the IRED, the driver circuit, and the thermal management design. A good design practice is to consider the minimum radiant intensity requirement of a system and the part to part tolerance. If the driving current is above 1.5 A, a pulsed operation is needed. A driver circuit with a switching regulator is usually preferred for high power IRED applications, given its high efficiency. Thus, it helps to improve the thermal performance of the end application.

Proper thermal management design is crucial to operating a high power IRED. The power dissipation in an IRED produces heat, which needs to be transferred to the ambient to prevent the junction temperature inside the IRED from reaching its maximum junction temperature. Therefore, a metal core PCB with high thermal conductivity is recommended for an application with a high power IRED. However, other PCB technology, such as FR4 PCB, can also be used. Although operation at a higher driving current and operating ambient temperature requires an improvement of the heat transfer by incorporating thermal design elements, such as thermal vias, enlarged solder pads, and a thicker copper layer. The DC and pulse derating diagrams for different PCB technologies and ambient temperatures, discussed in Chapters 4 and 5, can be used as guidance when selecting a suitable operating point when designing with a high power IRED.