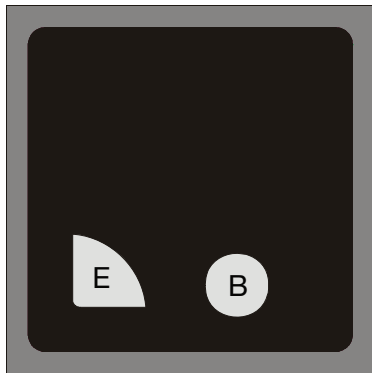


Silicon NPN Phototransistor



21682

FEATURES

- Package type: chip
- Package form: single chip
- Dimensions (L x W x H in mm): 0.72 x 0.72 x 0.22
- Wafer diameter (in mm): 100
- Radiant sensitive area (in mm²): 0.25
- High photo sensitivity
- Suitable for visible light
- Fast response times
- Angle of half sensitivity: $\phi = \pm 60^\circ$
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



DESCRIPTION

T1070P ambient light sensor chip is a silicon NPN epitaxial planar phototransistor. It is sensitive to visible light much like the human eye and has peak sensitivity at 570 nm.

GENERAL INFORMATION

The datasheet is based on Vishay optoelectronics sample testing under certain predetermined and assumed conditions, and is provided for illustration purpose only. Customers are encouraged to perform testing in actual proposed packaged and used conditions. Vishay optoelectronics die products are tested using Vishay optoelectronics based quality assurance procedures and are manufactured using Vishay optoelectronics established processes. Estimates such as those described and set forth in this datasheet for semiconductor die will vary depending on a number of packaging, handling, use, and other factors. Therefore sold die may not perform on an equivalent basis to standard package products.

APPLICATIONS

- Ambient light sensor
- Backlight dimmer

PRODUCT SUMMARY

COMPONENT	I_{PCE} (μA)	ϕ (deg)	$\lambda_{0.5}$ (nm)
T1070P	50	± 60	440 to 800

Note

- Test condition see table "Basic Characteristics"

ORDERING INFORMATION

ORDERING CODE	PACKAGING	REMARKS	PACKAGE FORM
T1070P-SD-F	wafer sawn on foil with disco frame	MOQ: 55 000 pcs	chip

Note

- MOQ: minimum order quantity

ABSOLUTE MAXIMUM RATINGS ($T_{amb} = 25^\circ C$, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Collector emitter voltage		V_{CEO}	6	V
Emitter collector voltage		V_{ECO}	1.5	V
Collector current		I_C	20	mA
Junction temperature		T_j	100	$^\circ C$
Operating temperature range		T_{amb}	-40 to +100	$^\circ C$
Storage temperature range		T_{stg1}	-40 to +100	$^\circ C$
Storage temperature range on foil		T_{stg2}	-40 to +50	$^\circ C$

BASIC CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Collector emitter breakdown voltage	$I_C = 0.1\text{ mA}$	$V_{(BR)CEO}$	6			V
Collector dark current	$V_{CE} = 5\text{ V}, E = 0$	I_{CEO}		3	50	nA
Collector emitter capacitance	$V_{CE} = 5\text{ V}, f = 1\text{ MHz}, E = 0$	C_{CEO}		16		pF
Collector light current	$E_V = 20\text{ lx}, \text{CIE illuminant A}, V_{CE} = 5\text{ V}$	I_{PCE}		10		μA
	$E_V = 100\text{ lx}, \text{CIE illuminant A}, V_{CE} = 5\text{ V}$	I_{PCE}		50		μA
Temperature coefficient of I_{PCE}	CIE illuminant A	TK_{IPCE}		1.18		%/K
	LED, white	TK_{IPCE}		0.9		%/K
Angle of half sensitivity		φ		± 60		deg
Wavelength of peak sensitivity		λ_p		570		nm
Range of spectral bandwidth		$\lambda_{0.5}$		440 to 800		nm
Collector emitter saturation voltage	$E_V = 20\text{ lx}, \text{CIE illuminant A}, I_{PCE} = 1.2\text{ }\mu\text{A}$	V_{CEsat}		0.1		V

Note

- The measurements are based on samples of die which are mounted on a TO-header without resin coating

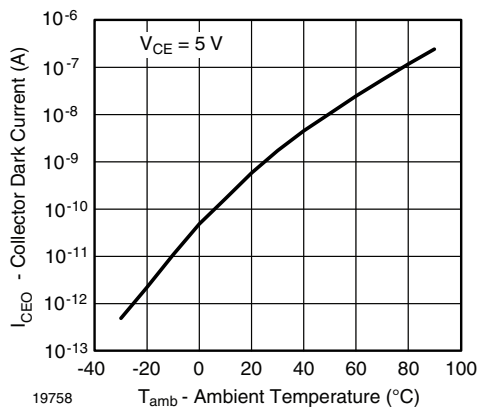
BASIC CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)


Fig. 1 - Collector Dark Current vs. Ambient Temperature

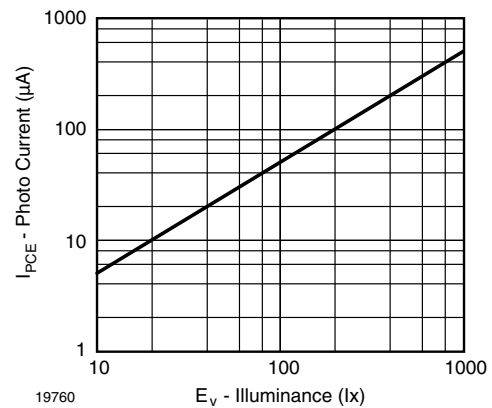


Fig. 3 - Photo Current vs. Illuminance

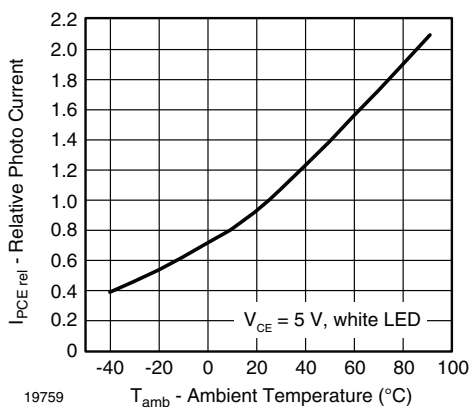


Fig. 2 - Relative Photo Current vs. Ambient Temperature

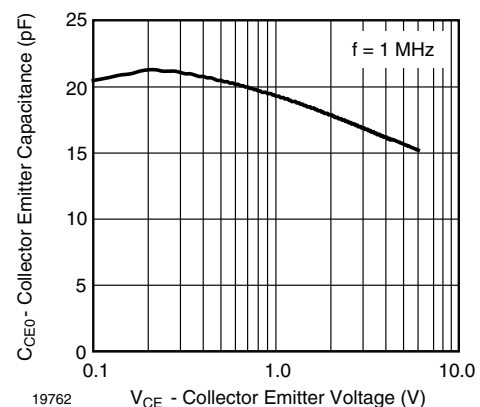


Fig. 4 - Collector Emitter Capacitance vs. Collector Emitter Voltage

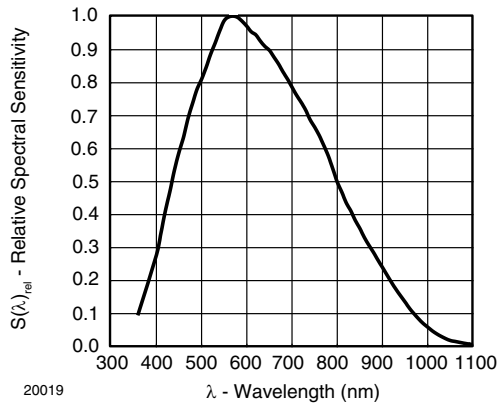


Fig. 5 - Relative Spectral Sensitivity vs. Wavelength

MECHANICAL DIMENSIONS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Length of chip edge (x-direction)	L_x		0.72		mm
Length of chip edge (y-direction)	L_y		0.72		mm
Sensitive area	A_S	0.5 x 0.5			mm ²
Die height	H		0.22		mm
Bond pad emitter (E)	a x b		0.1 x 0.1		mm ²

ADDITIONAL INFORMATION	
Frontside metallization, base (B), emitter (E)	aluminum
Backside metallization, collector	gold alloy
Dicing	sawing
Die bonding technology	epoxy bonding

Note

- All chips are checked in accordance with the Vishay Semiconductor, specification of visual inspection FVOV6870. The visual inspection shall be made in accordance with the "specification of visual inspection as referenced". The visual inspection of chip backside is performed with stereo microscope with incident light and 40x to 80x magnification. The quality inspection (final visual inspection) is performed by production. An additional visual inspection step as special release procedure by QM is not installed.

HANDLING AND STORAGE CONDITIONS

- The hermetically sealed shipment lots shall be opened in temperature and moisture controlled cleanroom environment only. It is mandatory to follow the rules for disposition of material that can be hazardous for humans and environment.
- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Singulated die are not to be handled with tweezers. A vacuum wand with non metallic ESD protected tip should be used.

PACKING

Chips are fixed on adhesive foil. Upon request the foils can be mounted on plastic frame or disco frame. For shipment, the wafers are arranged to stacks and hermetically sealed in plastic bags to ensure protection against environmental influence (humidity and contamination).

Use for recycling reliable operators only. We can help getting in touch with your nearest sales office. By agreement we will take back packing material, if it is sorted. You will have to bear the costs of transport. We will invoice you for any costs incurred for packing material that is returned unsorted or which we are not obliged to accept.



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