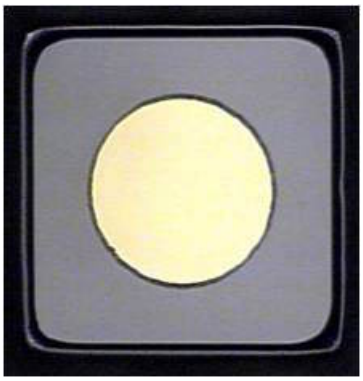
Specification of GaAlAs IR Emitting Diode Chip



FEATURES

- Package type: chip
- Package form: single chip
- Technology: multi quantum well (MQW)
- Dimensions chip (L x W x H in mm): 0.2 x 0.2 x 0.19
- Peak wavelength: λ = 940 nm
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

e4

RoHS COMPLIANT

HALOGEN FREE

GREEN (5-2008)

DESCRIPTION

TB9408VA is an infrared, 940 nm emitting diode in GaAlAs multi quantum well technology with high radiant power and high speed. Anode is the bond pad on top.

GENERAL INFORMATION

The datasheet is based on Vishay optoelectronics sample testing under certain predetermined and assumed conditions, and is provided for illustration purpose only. Customers are encouraged to perform testing in actual proposed packaged and used conditions. Vishay optoelectronics die products are tested using Vishay optoelectronics based quality assurance procedures and are manufactured using Vishay optoelectronics established processes. Estimates such as those described and set forth in this datasheet for semiconductor die will vary depending on a number of packaging, handling, use, and other factors. Therefore sold die may not perform on an equivalent basis to standard package products.

PRODUCT SUMMARY

COMPONENT	ϕ_e (mW)	I_e (mW/sr)	φ (deg)	λ_p (nm)	t_r (ns)
TB9408VA	3.5	4.0	± 80	940	15

Note

- Test condition see table “Basic Characteristics”

ORDERING INFORMATION

ORDERING CODE	PACKAGING	REMARKS	PACKAGE FORM
TB9408VA-SF-F	wafer sawn on foil	MOQ: 100 000 pcs	chip

Note

- MOQ: minimum order quantity

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Forward current		I_F	75	mA
Reverse voltage		V_R	5	V
Surge forward current	t_p = 100 µs	I_{FSM}	500	mA
Junction temperature		T_j	100	°C
Operating temperature range		T_{amb}	-40 to +85	°C
Storage temperature range chip		T_{stg1}	-40 to +100	°C
Storage temperature range on foil		T_{stg2}	-40 to +50	°C

BASIC CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)						
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Forward voltage	I_F = 5 mA	V_F	1.1	1.18	1.25	V
	I_F = 20 mA	V_F	1.13	1.26	1.4	V
	I_F = 100 mA	V_F		1.45		V
	I_F = 500 mA, t_p = 100 µs	V_F		2.0		V
Radiant power (1)	I_F = 100 mA	ϕ_e		22		mW
Radiant intensity (2)	I_F = 100 mA	I_e		4.0		mW/sr
Radiant power (epoxy encapsulated)	I_F = 100 mA	ϕ_e		40		mW
Radiant power chip (3)	I_F = 50 mA	ϕ_e	2.5	3.5	5.0	mW
Temperature coefficient of radiant power	I_F = 1 mA	$TK_{\phi e}$		-1.1		%/K
Reverse voltage	I_R = 10 µA	V_R	7	18		V
Temperature coefficient of forward voltage	I_F = 1 mA	TK_{VF}		-1.5		mV/K
Angle of half intensity	I_F = 100 mA	φ		> ± 80		deg
Peak wavelength	I_F = 30 mA	λ_p	920	945	960	nm
Spectral bandwidth	I_F = 30 mA	$\lambda_{0.5}$		25		nm
Rise time / fall time	I_F = 100 mA	t_r, t_f		15		ns

Notes

(1) The measurements are based on samples of die which are mounted on a TO-18 gold header without resin coating

(2) The radiant intensity, I_e, is measured on the geometric axis of the TO-18 header

(3) The radiant power, ϕ_e, is measured with chip on bare plate and aperture angle about 30°, as indicated on the label of each wafer

BASIC CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

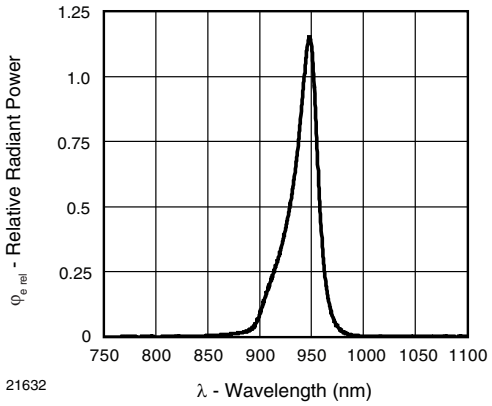


Fig. 1 - Relative Spectral Emission
$\phi_{e\ rel} = f(\lambda)$

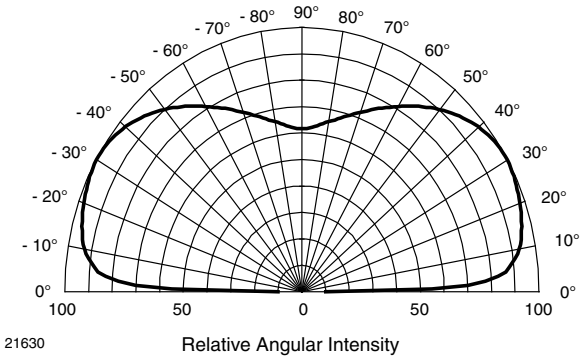


Fig. 2 - Radiant Characteristics
$I_{rel} = f(\varphi)$

DIMENSIONS

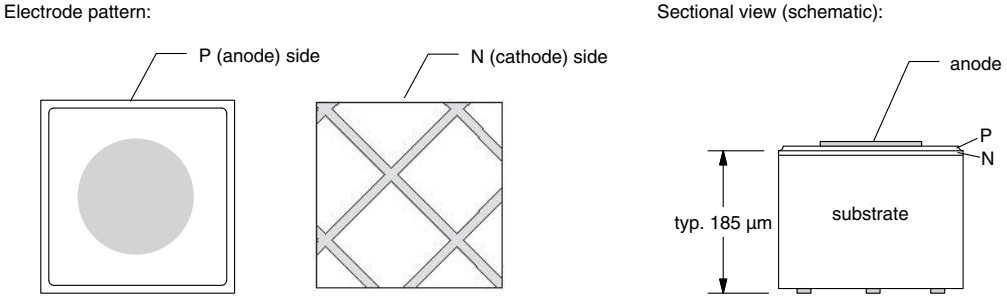


Fig. 3

MECHANICAL DIMENSIONS					
PARAMETER	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Length of chip edge (x-direction)	L_x	0.185	0.200	0.215	mm
Length of chip edge (y-direction)	L_y	0.185	0.200	0.215	mm
Emission area	A_E		0.18 x 0.18		mm^2
Die height	H	0.175	0.190	0.205	mm
Diameter of bondpad	d		0.110		mm

ADDITIONAL INFORMATION	
Frontside metallization, anode	gold
Backside metallization, cathode	gold alloy
Dicing	sawing
Die bonding technology	epoxy bonding

Note

- All chips are checked in accordance with the Vishay Semiconductor, specification of visual inspection FVOV6870.
  The visual inspection shall be made in accordance with the “specification of visual inspection as referenced”. The visual inspection of chip backside is performed with stereo microscope with incident light and 40x to 80x magnification.
  The quality inspection (final visual inspection) is performed by production. An additional visual inspection step as special release procedure by QM is not installed.

HANDLING AND STORAGE CONDITIONS

- The hermetically sealed shipment lots shall be opened in temperature and moisture controlled cleanroom environment only. It is mandatory to follow the rules for disposition of material that can be hazardous for humans and environment.
- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Singulated die are not to be handled with tweezers. A vacuum wand with non metallic ESD protected tip should be used.

PACKING

Chips are fixed on adhesive foil. Upon request the foils can be mounted on plastic frame or disco frame. For shipment, the wafers are arranged to stacks and hermetically sealed in plastic bags to ensure protection against environmental influence (humidity and contamination).

Use for recycling reliable operators only. We can help getting in touch with your nearest sales office. By agreement we will take back packing material, if it is sorted. You will have to bear the costs of transport. We will invoice you for any costs incurred for packing material that is returned unsorted or which we are not obliged to accept.

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