Optical Sensors | Application Note

Handling IR Emitters and Photo Detector Bare Die

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This application note provides instructions for how to handle and mount IR emitter and photo detector bare die products from Vishay. The application note additionally gives guidelines for unpacking, storage, and inspection of Vishay bare die products.

INTRODUCTION

Vishay produces chips from 2-, 3-, 4- and 6-inch wafers, which are sawn and delivered on loose foil (figure 1) or a disco frame (figure 2).

In case of loose foil, bad chips are removed and the measurement data is attached. In the case of disco frames, the foil is attached to a plastic wafer frame that is suitable for most automated die bonders (figure 2). Any unit marked with a black ink dot is considered to be a bad unit, and the label with the test data is attached.

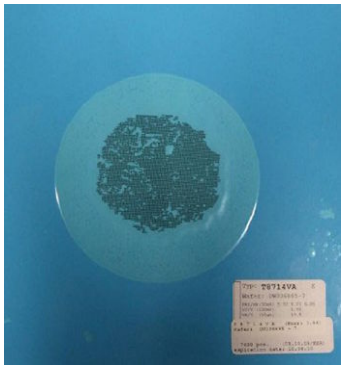

Fig. 1 - Sawn Dice on Loose Foil

Fig. 2 - Sawn Dice on Disco Frame

WAFER SHIPMENT

All wafers of a shipment are arranged in stacks that are packaged in hermetically sealed plastic bags to ensure protection against environmental influences such as humidity and contamination. The bags should be opened in clean rooms only and stored in a dark, nitrogen-filled cabinet after opening.

The label on each wafer will contain the part number, purchasing order number (if applicable), and lot and wafer numbers.

WAFER STORAGE

The storage temperature should be in the range of 19 °C to 26 °C: when stored properly, sawn wafers have a shelf life of approximately five years. If die are stored beyond this timeframe or under uncontrolled or inappropriate environmental conditions, picking problems at the die bonding stage (sticking die) or unreliable wire bonds due to corrosion of the bonding pads may occur.

WAFER INSPECTION

Up to 40 chips from each wafer are electrically tested to ensure that they comply with the datasheet limits.

The wafers are visually inspected to guarantee that all chips are free from defects. All chips are checked in accordance with the Vishay Semiconductors specification for visual inspection.

The visual inspection of the backside of the chip is performed with a stereo microscope with incident light and 40x to 80x magnification.

All chips are RoHS-compliant.

WAFER HANDLING

The surface of the wafer is very sensitive so special care should be taken when handling the wafer.

No cleaning is necessary, but the wafer should be opened in a temperature- and moisture-controlled cleanroom environment.

Products must be handled only on ESD-safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.

APPLICATION NOTE

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To avoid contamination and damage, wafers should never be handled by the bare fingers. Special vacuum tweezers are suitable for lifting the wafer by its edge (figure 3).

Fig. 3 - Lifting the Wafers with Vacuum Tweezers

Singulated die must not be handled with tweezers. A vacuum wand with a non-metallic ESD-protected tip should be used.

ATTACHING BARE DIE

To achieve the best performance, it is critical that special care be taken when mounting the die.

The most common form of die attach is conductive or non-conductive epoxy.

The maximum fillet height must be adopted to avoid the possibility of short circuits in case of conductive epoxy.

The die attach integrity should be checked by testing the shear strength according to MIL-STD-883.

WIRE BONDING OF BARE DIE

Thermosonic Au wire bonding or ultrasonic Al wire bonding are commonly used depending on the metallization of the die.

Customers working with Vishay bare die are advised to develop their own wire bonding parameters. Absolute bonding parameters for the chips cannot be specified due to variations in customer bonding equipment and materials.

The minimum size of the bond pads is 80 µm by 80 µm. The pad material is either aluminum or gold depending on the chip type.

The bond wire diameter should be chosen with respect to diameter of the bond pad region. The wire material should likewise be chosen with the bond pad material in mind (table 1).

TABLE 1

	Al pad	Au pad
Au wedge / ball	x	x
Al wedge	x	-

The wire bond integrity should be checked by testing the shear strength according to MIL_STD-750.

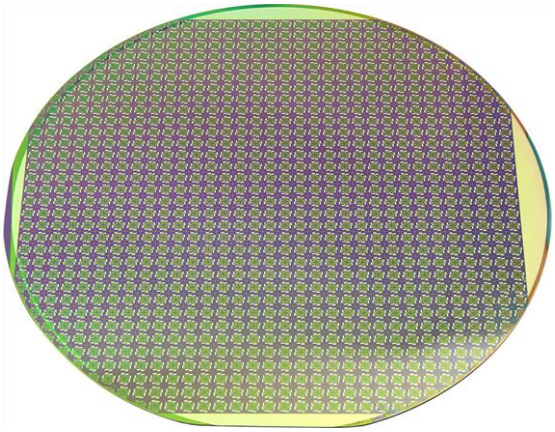

Fig. 4 - Nonsingulated Wafer

DISCLAIMER NOTE

Vishay produces high-quality chips that perform within the parameters of the datasheet. Typical performance values are not tested 100 % but they have been validated during qualification.

Vishay cannot guarantee that the die will function properly after mounting and post processing by the customer. It is the responsibility of the customer to test and to qualify the function of the chip in the final package.

The customer is responsible for the required knowledge to handle bare die and Vishay assumes no liability for consequential damages that may result in yield loss or field failures in the final application.