Optical Isolator for I²C Bus System

By Dimitrij Martins and Achim M. Kruck

INTRODUCTION

The I²C bus, also known as inter-IC bus, is a bidirectional, two-wire, multi-user bus, as shown in Fig. 1. It was developed by Philips Semiconductors [1] to connect micro controllers, EEPROMs, A/D and D/A converters, I/O interfaces, and other peripherals. The I²C bus consists of two lines: a serial data line (SDA) and a serial clock line (SCL). This serial bus has a data transfer rate of up to 100 kBit/s in the standard mode, up to 400 kBit/s in the fast mode, and up to 1 MBit/s in the fast mode plus. The 3.4 MBit/s high speed mode and the 5 MBit/s ultra fast mode are not considered in this application note, because they require either current-source pull-up circuits or are uni-directional.

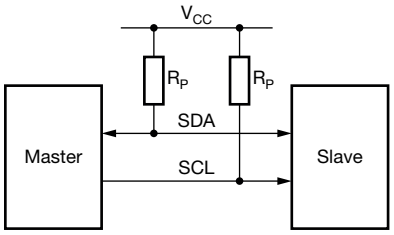

Fig. 1 - I²C Master / Slave Connection

A data transmission begins with a START (S) condition, a 7-bit slave address with the read / write designator (R/W), an acknowledge (ACK) bit, 8-bit data following the acknowledge (ACK) bit, and a STOP (P) condition, as shown in Fig. 2.

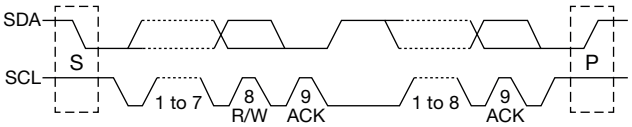

Fig. 2 - I²C Protocol

OPTICAL ISOLATION

For optical isolation between master and slave, an optocoupler is the perfect solution. Due to galvanic isolation, an optocoupler helps to break up ground loops and reduces the electrical noise due to optical light transmission across an isolation barrier.

It can restore the logic level and can be used for signal level transforming between different voltage level domains, e.g. from 5 V to 3.3 V or 24 V.

One channel is required for the serial clock line (SCL) and two channels for the serial data line (SDA) to transmit the data from master to slave and back.

DESIGN CONSIDERATIONS

The I²C bus is an active low data bus using open-collector (open-drain) outputs on master and slave.

When the serial data line (SDA) is pulled down to the logic “L” stage, a voltage divider is formed by the pull-up resistor (R_P), Schottky diode (D), and the internal phototransistor C-E junction. The output voltage (V_O) is the sum of the Schottky diode voltage drop (V_D) and the voltage drop of the phototransistor output (V_{OL}), as shown in Fig. 3.

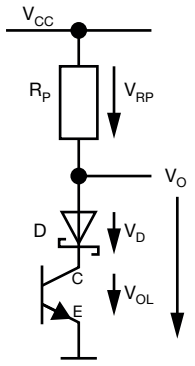

Fig. 3 - Voltage Divider

In the case of the bidirectional serial clock line (SCL), the diode D is not required. In this case, the voltage drop (V_D) will be set to 0. For the logic “H” stage, pull-up resistors (R_P, shown in Fig. 1) are required and can be calculated with the equation below:

$$R_P = \frac{V_{CC} - V_{OL} - V_D}{I_{OL}} \quad (1)$$

Note

[1] Reference to UM10204 I²C bus specification and user manual (now NXP Semiconductors): www.nxp.com/documents/user_manual/UM10204.pdf

APPLICATION NOTE

Optical Isolator for I²C Bus System

EXAMPLE CIRCUIT

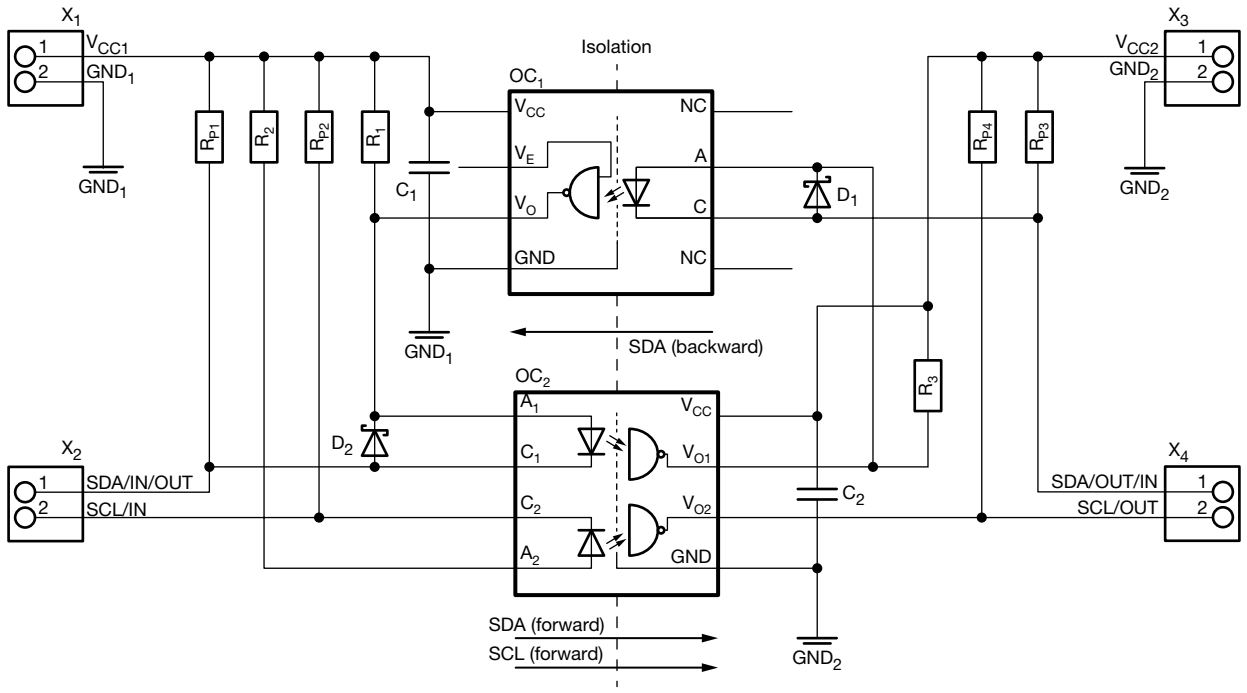

Fig. 4 - Example Schematic for Optical I²C Isolator

Fig. 4 depicts an exemplary optical I²C isolator circuit. Vishay's 10 MBd high speed optocouplers are used: a single channel VOH260A [1] for OC_1 (SDA (backward)) and a dual channel VOH263A [2] for OC_2 (SDA/SCL (forward)). Both are available in DIP-8 and SOIC-8 packages, named as VOIH060A [3] and VOIH063A [4].

By assuming that SDA/IN/OUT (X_2), SDA/OUT/IN (X_4), and SCL/IN (X_2) are at the logic "L" stage (saturation voltage drop of connected devices at X_2 and X_4 is neglected), the resistors R_1, R_2, and R_3 set the forward current (I_F) through the emitter LEDs of the optocoupler (OC_1, OC_2) inputs and can be calculated with the equations 2 and 3:

$$R_1 = R_2 = \frac{V_{CC1} - V_F}{I_F} \quad (2)$$

$$R_3 = \frac{V_{CC2} - V_F}{I_F} \quad (3)$$

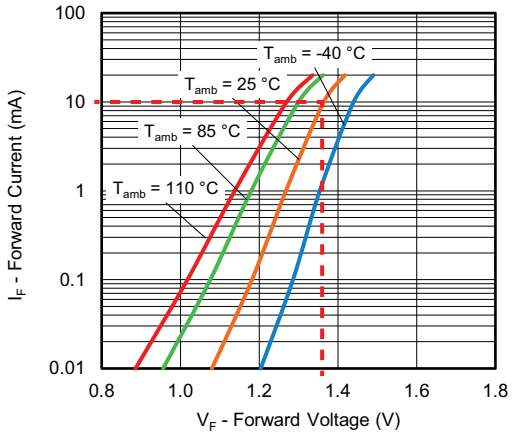

Fig. 5 - VOH260A Datasheet - V_F vs. I_F

According to the datasheet figure "Forward Voltage vs. Forward Current" [1], a voltage drop (V_F) of 1.35 V is caused by a forward current (I_F) of 10 mA through the input LED, as shown in Fig. 5.

Notes

(1) www.vishay.com/ppg?80354
(2) www.vishay.com/ppg?80355
(3) www.vishay.com/ppg?80356
(4) www.vishay.com/ppg?80357

Optical Isolator for I²C Bus System

By using 5 V as the supply voltage (V_{CC1}, V_{CC2}), values for R_1, R_2, and R_3 can be calculated using the equations 2 and 3:

$$R_1 = R_2 = \frac{5\ V - 1.35\ V}{10\ mA} = 365\ \Omega\ ^{(1)} \quad (4)$$

$$R_3 = \frac{5\ V - 1.35\ V}{10\ mA} = 365\ \Omega\ ^{(1)} \quad (5)$$

The capacitors C_1 and C_2 stabilize the power supply, and should be placed as close as possible to the optocouplers OC_1 and OC_2.

WORKING PRINCIPLE

SCL forward clock transmission:

When SCL/IN (X_2) is at the logic “H” stage, no forward current (I_F) is flowing through the emitter LED (A2/C2) and the optocoupler OC_2 output V_{O2} is also at the logic “H” stage.

When SCL/IN (X_2) is at the logic “L” stage, forward current (I_F) is flowing through the emitter LED (A2/C2) and the optocoupler OC_2 output V_{O2} is also at the logic “L” stage.

SDA forward data transmission:

When SDA/IN/OUT (X_2) is at the logic “H” stage, no forward current (I_F) is flowing through the emitter LED (A1/C1) and the optocoupler OC_2 output V_{O1} is also at the logic “H” stage.

When SDA/IN/OUT (X_2) is at the logic “L” stage, forward current (I_F) is flowing through the emitter LED (A1/C1). The optocoupler OC_2, output V_{O1}, and the anode A of the optocoupler OC_1 are at the logic “L” stage, so the emitter LED (A/C) is in reverse mode and bypassed by the diode D_1. Therefore, the emitter LED (A/C) is off and backward data transmission is blocked.

SDA backward data transmission:

When SDA/OUT/IN (X_4) is at the logic “H” stage, no forward current (I_F) is flowing through the emitter LED (A/C) and the optocoupler OC_1 output V_O is also at the logic “H” stage.

When SDA/OUT/IN (X_4) is at the logic “L” stage, forward current (I_F) is flowing through the emitter LED (A/C). The optocoupler OC_1, output V_O, and the anode A1 are at the logic “L” stage, so the emitter LED (A1/C1) is in reverse mode and bypassed by the diode D_2. Therefore the emitter LED (A1/C1) is off and forward data transmission is blocked.

RECOMMENDED BILL OF MATERIAL

TABLE 1 - OPTICAL I²C ISOLATOR

IDENTIFIER	COMMENT
X_1	Pin header, 2 circuits
X_2	Pin header, 2 circuits
X_3	Pin header, 2 circuits
X_4	Pin header, 2 circuits
R_1	365 Ω resistance
R_2	365 Ω resistance
R_3	365 Ω resistance
R_{P1}	1.5 kΩ resistance
R_{P2}	2.2 kΩ resistance
R_{P3}	1.5 kΩ resistance
R_{P4}	2.2 kΩ resistance
C_1	100 nF capacitance
C_2	100 nF capacitance
D_1	Low voltage drop Schottky diode
D_2	Low voltage drop Schottky diode
OC_1	10 MBd (single) high speed optocoupler VOH260A
OC_2	10 MBd (dual) high speed optocoupler VOH263A

CONCLUSION

It can be seen that by using the Vishay 10 MBd high speed optocoupler series it is easily possible to galvanically isolate I²C bus systems. Ground loops and electrical noise can be eliminated due to long term proven and robust optical isolation technology.

By choosing Vishay’s small and compact SOIC-8 package board space can be saved. The availability of a dual channel high speed optocoupler in one package provides additional board space savings.

Note

(1) The closest value to a norm series can be chosen