Soldering Recommendations for DFN Packages

By Henry Karrer

INTRODUCTION

The trend in automotive, industrial, and mobile applications towards reducing the package size and thickness of components is supported by Vishay Semiconductors, lead less packages (DFN) technology. The following guidelines are intended to help customers avoid trial and error in PCB design and reflow process tuning.

The following parameters are key to success:

- Using non solder mask defined (**NSMD**) solder lands
- Using the right amount of solder paste for proper stand-off and solder meniscus

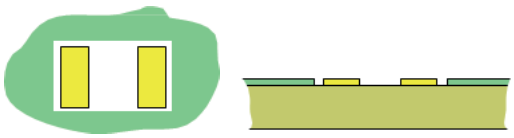
These packages allow customers to use automated optical inspection (AOI) of the solder joints, which pushes board-level reliability to the next level.

Using Vishay-recommended settings, board-level temperature cycle performance can meet JESD 22-A104 (-55 °C to +150 °C).

Customized tests (-40 °C to +125 °C) up to 5000 cycles were performed with positive results, too.

PCB SOLDER LAND DESIGN

The size of the solder lands is defined by the copper area (and its tolerances), with the effective solder land being equal to the copper area. The solder mask layer does not touch the solder lands; the typical solder mask layer offset must be at least 75 µm wider than the solder land. This value may vary depending on the class of PCB used. NSMD solder lands are recommended for DFN products.



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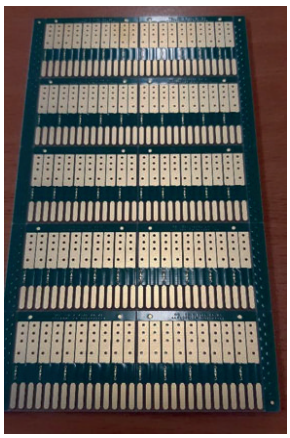
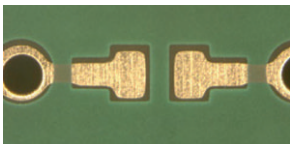
Soldering Recommendations for DFN Packages

Picture of Vishay test board (internal tests)





How to improve the temperature cycle performance of DFN products:

- Vishay internal tests showed that up to 5000 temperature cycles can pass without any electrical failure under the following test conditions:
  - Condition T min. = 40 °C, T max. = 125 °C
  - Cycle time: 20 min / 20 min
  - Dwell time

- Use Vishay-recommended footprint / copper pad. To use a copper footprint much larger than the recommended size (e.g. for cooling purpose) is not advised. The thermal mismatch between the PCB and the DFN will cause thermomechanical stress to the outer solder joint. A significant reduction of temperature cycle performance may be the result.

- **Solder Mask Defined (SMD) Solder Lands**
  A large copper area with a defined footprint by the solder mask is not recommended for DFN products.

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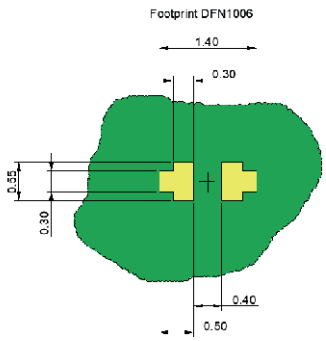
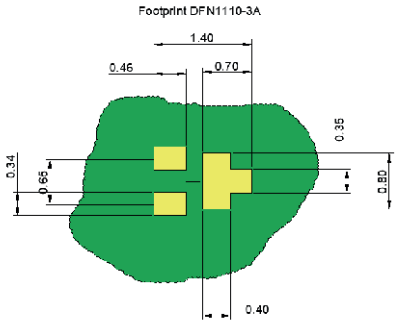
Soldering Recommendations for DFN Packages

FOOTPRINT (in millimeters) **FOR STENCIL THICKNESS OF 80 µm**

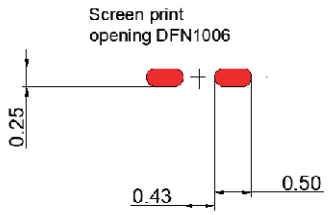
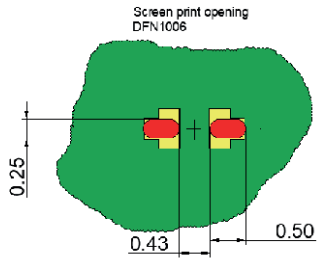
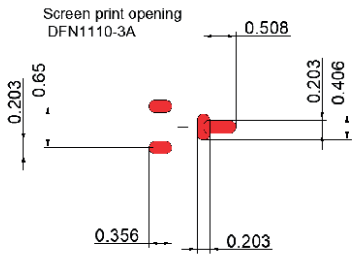
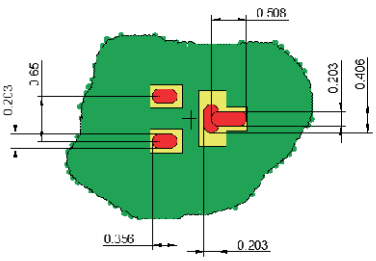


Footprint: DFN1006-2A, DFN1006-2B



Footprint: DFN1110-3A

SCREEN PRINT OPENING (in millimeters)

TABLE 1a: STENCIL SIZE FOR 80 µm STENCIL THICKNESS			
	LAND SIZE 1	**LAND SIZE 2**	
DFN1006-2A = DFN1006-2B	0.50 mm x 0.25 mm oblong	0.50 mm x 0.25 mm oblong	
			
DFN1110-3A	2 x 0.356 mm x 0.203 mm oblong	1 x 0.203 mm x 0.508 mm + 1 x 0.406 mm x 0.203 mm oblong	
			

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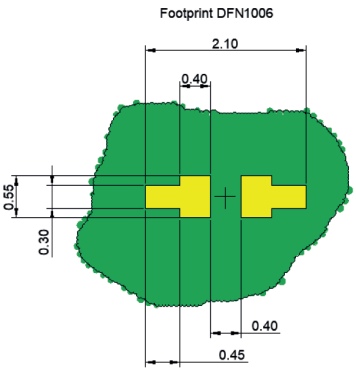
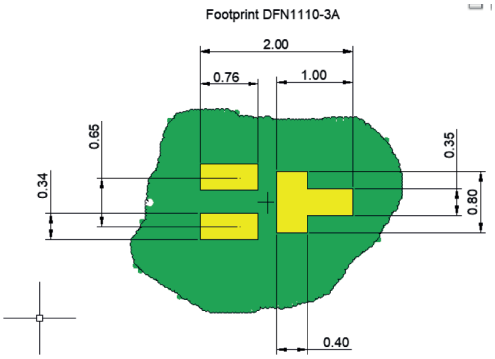
Soldering Recommendations for DFN Packages

FOOTPRINT (in millimeters) **FOR STENCIL THICKNESS OF 120 µm and longer solder meniscus**



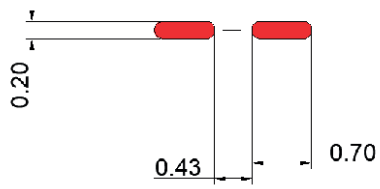
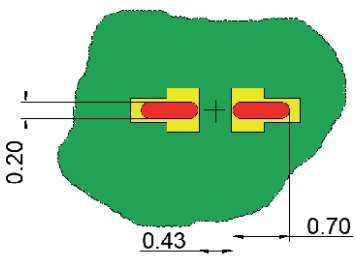
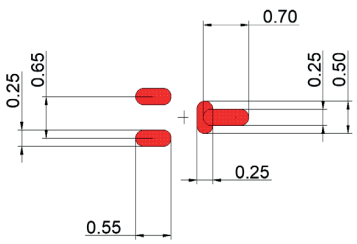
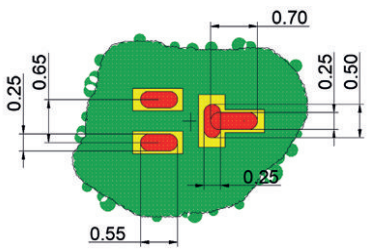
Footprint: DFN1006-2A, DFN1006-2B



Footprint: DFN1110-3A

SCREEN PRINT OPENING (in millimeters)

TABLE 1b: STENCIL SIZE FOR 120 µm STENCIL THICKNESS (and longer solder meniscus)

	LAND SIZE 1	LAND SIZE 2	
DFN1006-2A = DFN1006-2B	0.70 mm x 0.20 mm oblong	0.70 mm x 0.20 mm oblong	
	Screen print opening DFN1006 		
	2 x 0.55 mm x 0.25 mm oblong	1 x 0.25 mm x 0.50 mm + 1 x 0.70 mm x 0.25 mm oblong	
			

Depending on the customer's application (different size of other components requiring more / less solder paste), the stencil thickness may vary. Depending on the stencil thickness used, the stencil opening has to be adjusted to use the recommended amount of solder paste.

With an insufficient amount of solder paste, the lifetime of the solder joint will be affected.

With an excess of solder, AOI performance may be affected. In worst case scenario bridging solder will cause an electrical failure (short).

Screen Print Using a Stencil

Stencil screening of the solder paste onto the PCB is a common practice in the industry. Laser-cut openings with plasma treatment for good release of the solder paste are important features of the stencil in applying an accurate amount of solder paste onto the PCB.

Stencil thickness, openings, and opening design (radius) are all considerations in applying the right amount of solder paste onto the PCB.

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Soldering Recommendations for DFN Packages

RECOMMENDED SOLDER PASTE

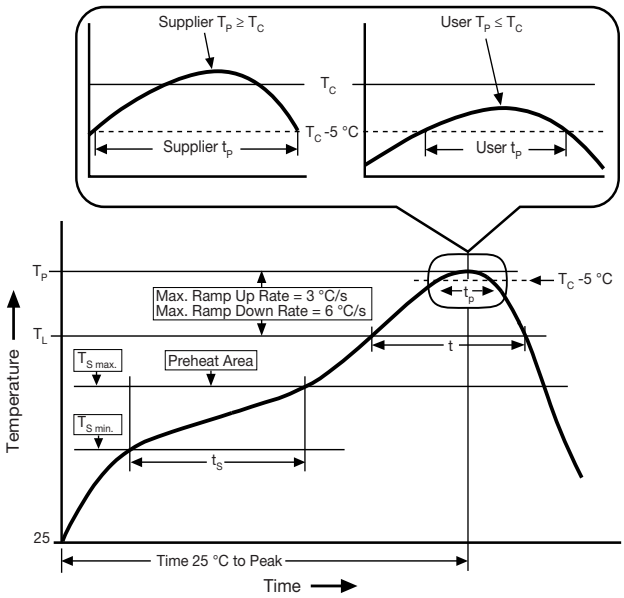
Stencil Screening

Use type 4 or higher (smaller ball size). In our evaluations we used the Cookson Electronics Alpha OM-338 CSP (96.5 % Sn / 3 % Ag / 0.5 % Cu) solder paste.

REFLOW SOLDERING PROCESS

A standard surface-mount reflow soldering process can be used (reference: JPC/JEDEC® J-STD-020E).

However, for an optimum process, recommendations from the solder paste supplier should be considered. Variations in chemistry and viscosity of the fluxer may require small adjustments to the soldering profile.



Reflow Soldering Profile according to JEDEC®-J-STD-020E

TABLE 3 - CLASSIFICATION PROFILES		
PROFILE FEATURE	**SnPb EUTECTIC ASSEMBLY**	**LEAD (Pb)-FREE ASSEMBLY**
PREHEAT AND SOAK		
Temperature min. ($T_{Smin.}$)	100 °C	150 °C
Temperature max. ($T_{Smax.}$)	150 °C	200 °C
Time (t_S) from ($T_{Smin.}$ to $T_{Smax.}$)	60 s to 120 s	60 s to 120 s
Average ramp-up rate ($T_{Smax.}$ to T_p)	3 °C/s max.	
Liquidus temperature (T_L)	183 °C	217 °C
Time (t_L) to liquidus	60 s to 150 s	60 s to 150 s
Peak package temperature (T_p) (1)	see classification temperature in table 3	see classification temperature in table 4
Time (t_p) (2) with 5 °C of the specified classification temperature (T_C)	20 s (2)	30 s (2)
Average ramp-down rate (T_p to $T_{Smax.}$)	6 °C/s max.	
Time 25 °C to peak temperature	6 min max.	8 min max.

Notes

(1) Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum

(2) Tolerance for time at peak profile temperature (T_p) is defined as a supplier minimum and user maximum

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Soldering Recommendations for DFN Packages

Notes

1. All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g. live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e. dead-bug), T_p shall be within ± 2 °C of the live-bug T_p and still meet the T_C requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperature refer to JEP140 for the recommended thermocouple use
2. Reflow profiles in this document are for classification / preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in this table. For example, if T_C is 260 °C and time t_p is 30 s, this means the following for the supplier and the user:
   - For a supplier: the peak temperature must be at least 260 °C. The time above 255 °C must be at least 30 s
   - For a user: the peak temperature must not exceed 260 °C. The time above 255 °C must not exceed 30 s
3. All components in the test load shall meet the classification profile requirements
4. SMD packages classified to a given moisture sensitivity level by using procedures or criteria defined within any previous version of J-STD-020, JESD22-A112 (rescinded), or IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired

TABLE 4 - SnPb EUTECTIC PROCESS - CLASSIFICATION TEMPERATURES (T_C)

PACKAGE THICKNESS	VOLUME mm^3 < 350	VOLUME mm^3 ≥ 350
< 2.5 mm	235 °C	220 °C
≥ 2.5 mm	220 °C	220 °C

TABLE 5 - LEAD (Pb)-FREE PROCESS - CLASSIFICATION TEMPERATURES (T_C)

PACKAGE THICKNESS	VOLUME mm^3 < 350	VOLUME mm^3 350 to 2000	VOLUME mm^3 > 2000
< 1.6 mm	260 °C	260 °C	260 °C
1.6 mm to 2.5 mm	260 °C	250 °C	245 °C
> 2.5 mm	250 °C	245 °C	245 °C

Notes

5. At the direction of the device manufacturer, but not the board assembler / user, the maximum peak package body temperature (T_p) can exceed the values specified in Tables 2 and 3. The use of a higher T_p does not change the classification temperature (T_C)
6. Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and / or non-integral heatsinks
7. The maximum component temperature reached during reflow depends on package thickness and volume. The use on convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist
8. Moisture sensitivity levels of components intended for use in a lead (Pb)-free assembly process shall be evaluated using the lead (Pb)-free classification temperatures and profiles defined in Tables 4-1 and 4-2, whether or not lead (Pb)-free
9. SMD packages classified to a given moisture sensitivity level by using procedures or criteria defined within any previous version of J-STD-020, JESD22-A112 (rescinded), or IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired

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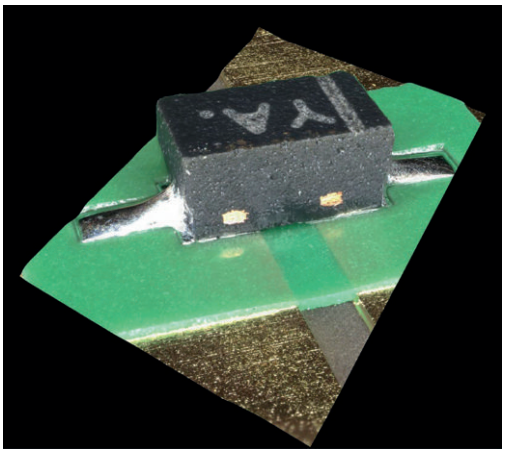
Soldering Recommendations for DFN Packages

AOI CAPABLE

The solderable sidewall / flanks (with guaranteed Sn plating thickness, same as on bottom side) enable customers to use automated optical inspection (AOI) with camera instead of X-ray system. With a proper PC board footprint design (extended on both sides) and right amount of solder paste, a homogenous solder meniscus will be formed after reflow soldering.

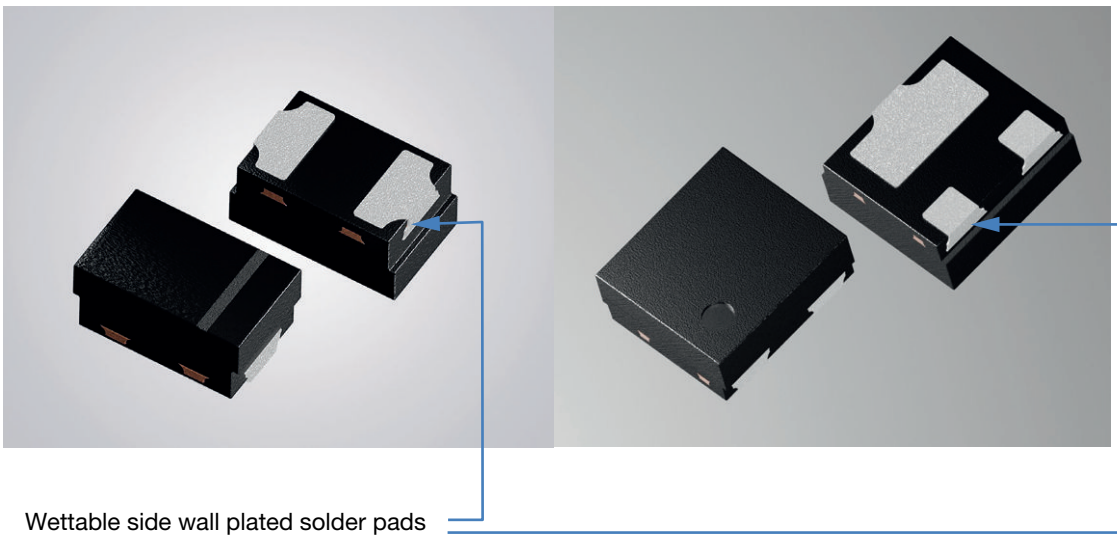
This solder meniscus can be inspected / measured with an optical camera system to judge for proper soldering result.

Sketch of solder meniscus



Real picture of DFN after reflow soldering showing meniscus

WETTABLE SIDEWALL PLATED SOLDER PADS ON DFN1006 AND DFN1110



Wettable side wall plated solder pads

- Side-wettable flanks for easy automated optical inspection (AOI)
- Robust solder joints, high reliability

REWORK PROCEDURE

For rework, the DFN package must be removed from the PCB if there is any issue with the solder joints. Standard SMT rework systems are recommended for this. Due to the small size of the package, the rework system should be equipped with a proper magnification aid.

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