



# How to Use an SiC Diode in a PFC Circuit

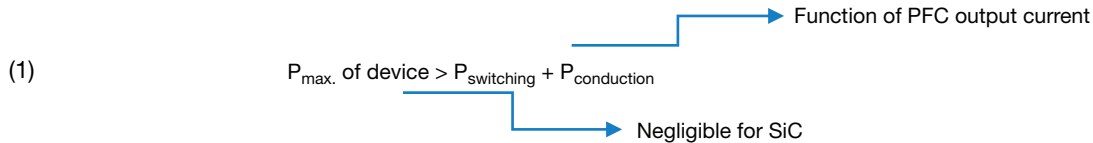
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## INTRODUCTION

An SiC diode is the optimal choice for power factor correction (PFC) operated under continuous conduction mode because its particular reverse recovery characteristic reduces switching losses to almost zero.

The selection criteria for an SiC diode are different from those for an Si diode in the same circuit. Usually at high frequencies in CCM, Si diodes show switching losses that are not negligible. The current capability of each diode is defined as the DC current that in a certain thermal condition brings the  $T_J$  to its limit; normally 175 °C for an SiC diode and 150 °C to 175 °C for an Si diode.

The diode's current capability is related to the maximum power that the diode can manage, evaluated only with DC current. However, a PFC diode is switching, so the device should be able to manage all dissipated power, not only conduction losses.



## BASICS OF ACTIVE PFC CIRCUITS

Active PFC has become quite common in AC/DC switch mode power supplies. For power supplies with output power ratings higher than 300 W, the harmonics and consequently its reactive power, loaded from the grid should be lower than the value specified in IEC61000-4-3. To meet this requirement, the input stage requires active PFC rather than a simple rectifier bridge along with a capacitor.

A typical active PFC circuit made with a boost converter is shown in Fig. 1.

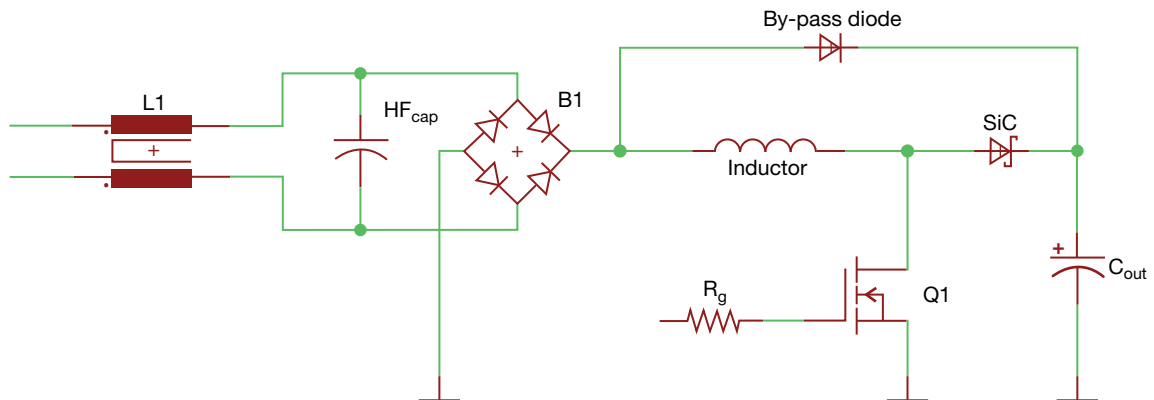


Fig. 1 - A Typical Active PFC Stage Implemented With a Boost Converter

APPLICATION NOTE

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The boost converter can work in three different modes: discontinuous current mode (DCM), critical current mode (CrCM), and continuous current mode (CCM). These terms are named from the shape of the current each through the inductor that contributes different stresses on the diode as shown in Fig. 2.

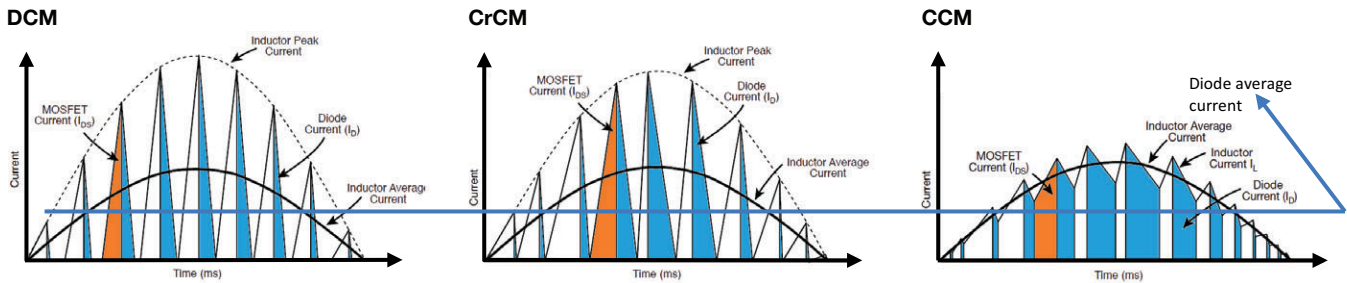


Fig. 2 - Instantaneous and Average Current in a PFC Boost Circuit

In DCM or CrCM, since the current from the inductor through the diode reaches zero before the switch Q1 turns on, the turn-off of the diode is not stressful and the associated switching loss is very low. Therefore, for PFC under DCM or CrCM, the switching loss's difference between Si and SiC diodes is subtle. Most of their losses are related to conduction behavior rather than the switching characteristic. As a result, in DCM or CrCM, an Si diode would basically be preferable because the forward voltage at high current is lower than the forward voltage of a comparable SiC diode, as shown in Fig. 3.

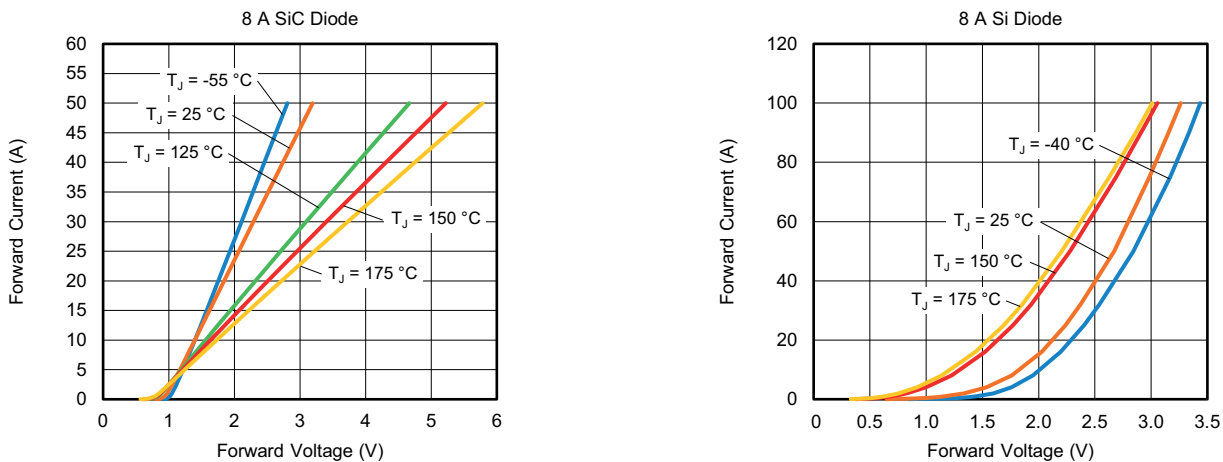


Fig. 3 - SiC and Si Diode Forward Voltage Comparison

Fig. 2 shows how the inductor current changes along with the mode we choose in the PFC boost circuit. It is true that switching loss from reverse recovery of the diode in DCM is negligible. However, its peak current would be much greater than that in CCM with the same output average current.

As the required output power goes higher, the peak current under DCM or CrCM proportionally goes up which induces some side effects.

The first is that the higher peak current would saturate the inductor. As a result, circuits designers should use a bigger inductor which reserves more margin to keep the inductor from saturation but requires more space and expense.

Plus, the higher ripple current results from the higher peak current requires a better filter in the input to avoid injecting high frequency noise into the grid. For example, in Fig. 1 the  $HF_{cap}$  should be smaller in CCM than in DCM / CrCM circuits.

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Consequently, CCM is preferable for high power circuits because it reduces the space and expense. However, at diode turn-off in CCM there is large switching loss in the diode. These losses are due to the reverse recovery current of the stored charge in the Si diode. Therefore, the choice of Si diode in a CCM circuit generally requires a device with greater average forward current capability than needed. Besides, the active switch (Q1 in Fig. 1) should also be carefully chosen to manage losses induced from the stored charge of the diode.

An SiC diode is competent in the CCM circuits because its reverse recovery current is mainly capacitive.

The switching loss in the SiC diode will be near zero because the minority carrier injection is little. Plus, the reverse recovery current peak is so small that the turn-on switching loss in the active switch is much lower than the loss of the comparable Si diode. The improvement on the decrease of switching loss benefits the reduction in chip size and expense not only in diode but also in the active switch.

### CHARACTERISTICS OF SiC SCHOTTKY BARRIER DIODE

The breakdown capability of a diode, its Schottky or PN junction, is related to the critical electric field which is proportional to the square of the semiconductor's energy gap,  $E_g$ , as shown in Fig. 4. The SiC diode has an  $E_g$  around 3.2 eV, while the pure Si diode has an  $E_g$  around 1.1 eV.

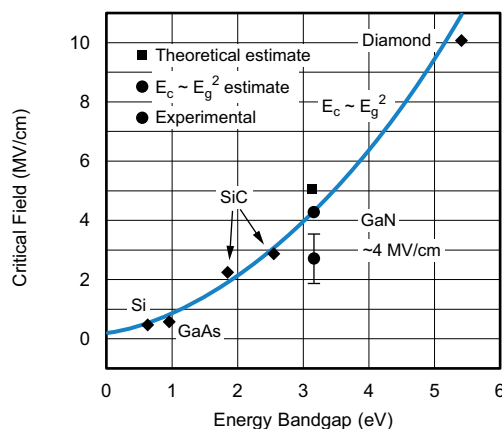


Fig. 4 - Energy Gap vs. Critical Electric Field

Based on this characteristic, the pure Si Schottky junction, even though it is adequate in fast switching, is tolerable to work under a maximum reverse voltage of around 150 V. Some specialized structure would extend this limitation to 200 V. For breakdown voltage higher than 200 V, it would be achieved with much sacrifice in the forward voltage drop that makes the usage of Si Schottky junction meaningless. On the contrary, for a pure SiC Schottky junction, the reverse voltage capability could be higher than 700 V. As a result, it is feasible to build a Schottky diode with high voltage breakdown using SiC substrate.

Building a SiC diode with a pure Schottky junction is attainable with the advantage of the lowest possible forward voltage. However, it is vulnerable to the surge current that is common in the PFC application.

For example, during the startup, short over current are quite common that could damage the SiC pure Schottky diode. Besides, PFC is a non-isolated converter that any abnormalities in the input can directly transfer to the output through the diode with dangerous overstress.

Vishay compromises this deficiency by implementing a special MPS structure that keeps the forward voltage under control during high current situation. This solution provides a high surge current capability for a 10 ms sinusoidal pulse and increasing diode reliability for currents with high crest factor.

As shown in Fig. 5, the MPS structure has a portion of the Schottky contact area replaced with the PN junction that help the increase of the conductivity of the drift zone at high current that keeps the forward voltage at low value as in Fig. 6.

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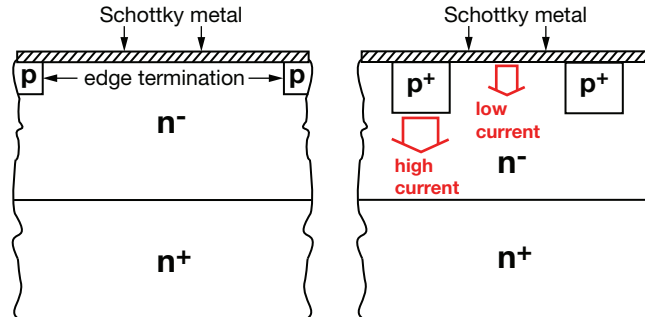


Fig. 5 - SiC Schottky Diode (left) and SiC MPS Diode (right) <sup>(1)</sup>

The PN junction has a higher threshold voltage than the Schottky junction. The adding of PN area reduces the Schottky area results in a diode mixed with unipolar and bipolar characteristics. This results in an SiC diode with a smaller Schottky contact area that increases the forward voltage at low forward current.

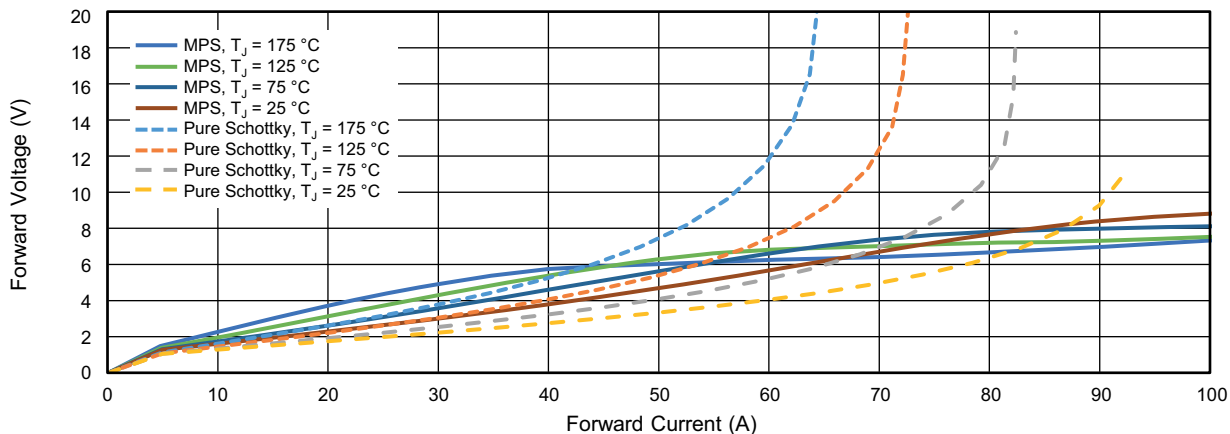


Fig. 6 - Forward Voltage Comparison between MPS and Pure Schottky Structure

Fig. 6 shows the IV curve of pure Schottky and MPS diodes under different temperatures with the same die size. The SiC diode with MPS structure has a steadier forward voltage at high forward current that goes down with temperature. The one with pure Schottky structure has lower forward voltage at low forward current but the forward voltage rises steeply at high forward current.

Vishay utilizes an improved version of the MPS structure to minimize the dramatic growth in the forward voltage at high current without compensating too much the forward voltage at low current.

From this application point of view, the improved surge capability could potentially suggest the removal of the bypass diode between the input and DC capacitor in Fig.1. However, for high power applications where the DC capacitor would be large, bypass diode is still needed for better reliability. Plus, in some applications where the PFC inductance is large, it is possible that the transient voltage at the C<sub>out</sub> capacitor during power-on would be too large without the help of the bypass diode.

Basically, Si diode could endure current surge that is 30 times higher than its average current. For SiC diode, this rate is around 5 times mainly because its VF's positive temperature characteristic.

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### POWER LOSSES MODEL

There are three power losses in a diode. Conduction, switching, and leakage power losses.

#### Leakage Power Loss

For the leakage power loss, it is negligible since Vishay's devices have the leakage current below 10 μA at high temperatures up to 175 °C, which is pretty low. For example, the VS-3C08ET07T-M3 has typical leakage of around 2 μA at 175 °C and 650 V that contributes only 1.3 mW which is insignificant.

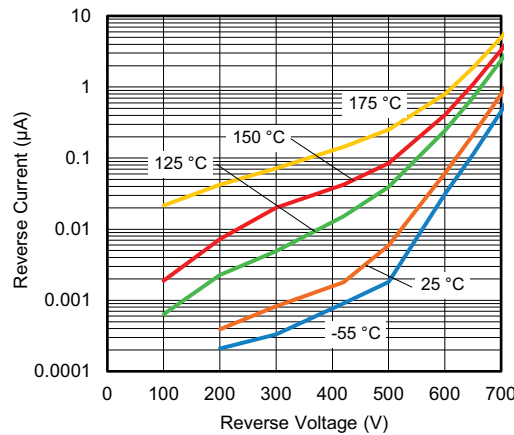


Fig. 7 - Typical Leakage of the VS-3C08ET07T-M3 as a Function of Reverse Voltage and Temperature

#### Conduction Power Loss

Generally, the major source of power losses in the diode is the conduction loss. The evaluation of conduction loss is straightforward based on the definition of average power:

$$(2) \quad P_{avg} = \frac{1}{T} \int_0^T v_F(t) i_F(t) dt$$

Given that we recorded the test waveform, the result could be conducted using the numerical method.

However, it is not applicable if we do not know the waveform beforehand or the waveform itself is hard to be operated. Plus, the nonlinear exponential relation between  $i_F$  and  $V_F$  also makes it hard to use:

$$(3) \quad i_F(V_F, T_J) = I_S(T_J) \left( e^{\frac{qV_F}{nKT_J}} - 1 \right)$$

Therefore, a simplified, linear, and user-friendly formula is suggested to approach the reality:

$$(4) \quad v_F(T_J, i_F(t)) = V_{to}(T_J) + R_d(T_J) i_F(t)$$

$V_{to}$  is the turn on voltage and  $R_d$  is the diode resistance. It is noticeable that the simplified  $V_F$  differs from the real  $V_F$  to some degree at the given  $i_F$ . Therefore, it is formulated not for the evaluation of  $V_F$  but for that of the power consumption. The relation between the real IV curve and the simplified model are in Fig. 8.

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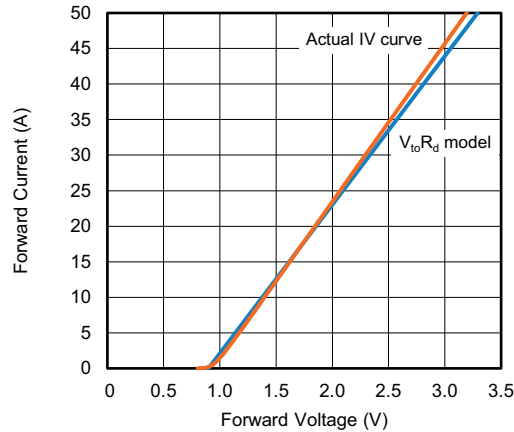


Fig. 8 - Actual IV Curve vs.  $V_{to}R_d$  Model

Suppose that the  $T_J$  reaches equilibrium and its variation along with time is negligible. The average power could be calculated:

$$(5) \quad P_{avg} = \frac{1}{T} \int_0^T v_F(T_J, i_F(t)) \times i_F(t) dt = V_{to}(T_J) \times \frac{1}{T} \int_0^T I_F(t) dt + R_d(T_J) \times \frac{1}{T} \int_0^T I_F^2(t) dt = V_{to}(T_J) \times I_{F\_avg} + R_d(T_J) \times I_{F\_RMS}^2$$

With the average power derived above using the wildly picked  $T_J$ , iteratively modifying the  $T_J$  chosen to accommodate the  $P_{avg}$  and the thermal characteristics of the system to approach the best solution for this model.

The relations of  $V_{to}$  and  $R_d$  along with  $T_J$  are pretty linear, thanks to good behavior with temperature of Gen 3 diode, as shown:

$$(6) \quad V_{to}(T_J) = k_V(T_J - 25) + V_{to}(25 \text{ } ^\circ\text{C})$$

$$(7) \quad R_d(T_J) = k_R(T_J - 25) + R_d(25 \text{ } ^\circ\text{C})$$

For Vishay's SiC Gen 3 devices the coefficients are given in the following table:

<b>TABLE 1 - <math>V_{to}R_d</math> MODEL'S PARAMETERS FOR VISHAY'S GEN 3 SiC DIODE</b>				
<b>PART NUMBER</b>	<b><math>V_{to}</math> (V)</b>	<b><math>R_d</math> (<math>\Omega</math>)</b>	<b><math>k_V</math> (V/<math>^\circ</math>C)</b>	<b><math>k_R</math> (<math>\Omega</math>/<math>^\circ</math>C)</b>
VS-3C04ET07T-M3, VS-3C04ET07S2L-M3	9.419E-01	9.520E-02	-1.131E-03	6.021E-04
VS-3C06ET07T-M3, VS-3C06ET07S2L-M3	9.428E-01	6.670E-02	-1.152E-03	4.061E-04
VS-3C08ET07T-M3, VS-3C08ET07S2L-M3, VS-3C16CP07L-M3	9.368E-01	4.810E-02	-1.155E-03	3.123E-04
VS-3C12ET07T-M3, VS-3C12ET07S2L-M3	9.401E-01	3.268E-02	-1.105E-03	1.843E-04
VS-3C16ET07T-M3, VS-3C16ET07S2L-M3	9.410E-01	2.413E-02	-1.180E-03	1.541E-04
VS-3C10ET07T-M3, VS-3C10ET07S2L-M3, VS-3C20CP07L-M3	9.372E-01	3.643E-02	-1.166E-03	2.236E-04
VS-3C20ET07T-M3, VS-3C20ET07S2L-M3, VS-3C40CP07L-M3	9.400E-01	2.014E-02	-1.216E-03	1.336E-04

In the PFC circuits, the average current through the diode is:

$$(8) \quad I_{d\_avg} = \frac{P_{out}}{V_{out}}$$

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For RMS current in CCM, an accurate model is quoted: <sup>(3)</sup>

$$(9) \quad I_{d_{RMS}} = \sqrt{\frac{16}{3\pi} \times \frac{P_{in}^2}{V_{pk} V_{out}} + \frac{1}{9\pi} \times \frac{T_S^2 V_{pk}^3}{L_{pfc}^2 V_{out}} - \frac{1}{16} \times \frac{T_S^2 V_{pk}^4}{L_{pfc}^2 V_{out}^2} + \frac{4}{45\pi} \times \frac{T_S^2 V_{pk}^5}{L_{pfc}^2 V_{out}^3}}$$

$P_{out}$  = PFC output power in Watt

$P_{in}$  = PFC input power in Watt

$V_{out}$  = PFC output voltage in Volt

$V_{pk}$  = PFC AC input voltage peak in Volt

$T_S$  = PFC switching period in second

$L_{pfc}$  = PFC inductance in Henry

Supposed that the ripple current is small enough which means the PFC inductor is big enough or the switching frequency is high enough, the  $I_{d_{RMS}}$  could be approximated to:

$$(10) \quad I_{d_{RMS}} = P_{in} \times \sqrt{\frac{16}{3\pi} \times \frac{1}{V_{pk} V_{out}}} = \frac{P_{out}}{\eta} \times \sqrt{\frac{16}{3\pi} \times \frac{1}{V_{pk} V_{out}}}$$

Where  $\eta$  is the estimated efficiency of the converter.

This simplified approximation is good enough for diode's selection.

With these coefficients, a preliminary evaluation of the dissipated power could be achieved.

### EXAMPLE OF EVALUATION

To summarize, evaluating the power loss of an SiC diode using only the conduction loss based on its junction temperature is sufficient since its reverse loss and switching loss are negligible.

For example:

- 3 kW PFC
- $V_{in}$ : 230 V<sub>AC</sub>
- $V_{out}$ : 370 V<sub>DC</sub>
- $F_{sw}$ : 30 kHz

Assume the efficiency is good enough so that  $P_{in} \approx P_{out}$  for the ease of calculation.

The first step is to evaluate the  $I_{d_{avg}}$  and  $I_{d_{RMS}}$  using formula (8) and (10) respectively:

$$I_{d_{avg}} = \frac{3000 \text{ W}}{370 \text{ V}} = 8.11 \text{ A}$$

$$I_{d_{RMS}} = 3000 \text{ W} \times \sqrt{\frac{16}{3\pi \times 370 \text{ V} \times 230 \sqrt{2} \text{ V}}} = 11.24 \text{ A}_{RMS}$$

With an average current around 8 A, the first tentative choice could be VS-3C10ET07T-M3, where its  $I_{F(AV)}$  is 10 A.

The second step is to evaluate the power losses in the diode with formula (5) using  $V_{to}$  and  $R_d$  around 25 °C:

$$P_d = V_{to} \times I_{d_{avg}} + R_d \times I_{d_{RMS}}^2 = 0.937 \text{ V} \times 8.11 \text{ A} + 0.036 \text{ } \Omega \times 11.24 \text{ A}^2 \approx 12.2 \text{ W}$$

The VS-3C10ET07T-M3 has a thermal resistance  $R_{thJC} = 1.8 \text{ } ^\circ\text{C/W}$ . Assuming the case temperature is 80 °C, the junction temperature  $T_J$  is around  $80 + 1.8 \times 12.2 = 101.96 \text{ } ^\circ\text{C}$ .

The third step is to evaluate the power loss again using  $V_{to}$  and  $R_d$  at  $T_J = 101.96 \text{ } ^\circ\text{C}$ .

The renewed evaluation of the power loss is 13.65 W which results in a more accurate  $T_J = 104.57 \text{ } ^\circ\text{C}$ . Use the above methods iteratively after the difference between the last two outcomes is within 1 °C.



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Note that in a real evaluation the case temperature could change because of a change in the thermal load of the heatsink. From this preliminary evaluation, a 3 kW PFC implemented with the VS-3C10ET07T-M3 has 12.2 W of losses in the boost diode. To keep the junction temperature at 105 °C which is a safe operation point for SiC diode, a heatsink is required with a thermal resistance case to ambient  $R_{thCA}$  around 2.92 °C/W, considering an ambient of 40 °C. Another trial using VS-3C08ET07T-M3 could be done to see if it is possible to implement a diode with smaller chip size. The result is 16.46W with  $T_J = 117.6$  °C,  $T_C = 88$  °C and  $T_A = 40$  °C. The resulting  $T_J$  and  $T_C$  are higher than the value obtained with VS-3C10ET07T-M3 but absolutely safe.

### CONCLUSION

The preliminary choice of a SiC diode for a PFC circuit is attainable using the measures introduced.

Since the reverse and switching loss are negligible, the evaluation of conduction loss requires only a few steps using the data in Table 1. The amount of the PFC output current is enough to pick up one or two devices for engineers to do the preliminary test in their prototypes.

### REFERENCES

- (1) Adapted from Fig. 6.10 in Semiconductor Power Devices: Physics, Characteristics, Reliability; Lutz, J., Schlangenotto, H., Scheuermann, U., De Doncker, R., Springer
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