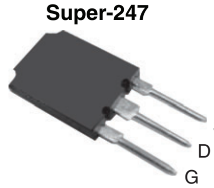
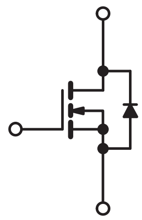
Power MOSFET

Super-247





N-Channel MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	600	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.110
Q_g (Max.) (nC)	330	
Q_{gs} (nC)	84	
Q_{gd} (nC)	150	
Configuration	Single	

FEATURES

- Low gate charge Q_g results in simple drive requirement
- Improved gate, avalanche and dynamic dV/dt ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Enhanced body diode dV/dt capability
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Hard switching primary or PFC switch
- Switch mode power supply (SMPS)
- Uninterruptible power supply
- High speed power switching
- Motor drive

ORDERING INFORMATION	
Package	Super-247
Lead (Pb)-free and halogen-free	SiHFPS40N60K-GE3

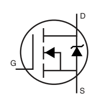
ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	600	V
Gate-source voltage			V_{GS}	± 30	
Continuous drain current	V_{GS} at 10 V	T_C = 25 °C	I_D	40	A
		T_C = 100 °C		24	
Pulsed drain current [a]			I_{DM}	160	
Linear derating factor				4.5	W/°C
Single pulse avalanche energy [b]			E_{AS}	600	mJ
Repetitive avalanche current [a]			I_{AR}	40	A
Repetitive avalanche energy [a]			E_{AR}	57	mJ
Maximum power dissipation	T_C = 25 °C		P_D	570	W
Peak diode recovery dV/dt [c]			dV/dt	7.5	V/ns
Operating junction and storage temperature range			T_J, T_{stg}	- 55 to + 150	°C
Soldering recommendations (peak temperature)	for 10 s			300 [d]	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Starting T_J = 25 °C, L = 0.84 mH, R_g = 25 Ω, I_{AS} = 38 A, dV/dt = 5.5 V/ns (see fig. 12a)
c. $I_{SD} \leq 38$ A, dI/dt ≤ 150 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C
d. 1.6 mm from case

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	40	°C/W
Case-to-sink, flat, greased surface	R_{thCS}	0.24	-	
Maximum junction-to-case (drain)	R_{thJC}	-	0.22	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	600	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.63	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	3.0	-	5.0	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 30 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 600 V, V_{GS} = 0 V	-	-	50	μA
		V_{DS} = 480 V, V_{GS} = 0 V, T_J = 125 °C	-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 10 V; I_D = 24 A [b]	-	0.110	0.130	Ω
Forward transconductance	g_{fs}	V_{DS} = 50 V, I_D = 24 A [b]	21	-	-	S
Dynamic						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5	-	7970	-	pF
Output capacitance	C_{oss}		-	750	-	
Reverse transfer capacitance	C_{rss}		-	75	-	
Output capacitance	C_{oss}	V_{GS} = 0 V; V_{DS} = 1.0 V, f = 1.0 MHz	-	9440	-	
		V_{GS} = 0 V; V_{DS} = 480 V, f = 1.0 MHz	-	200	-	
Effective output capacitance	C_{oss} eff.	V_{GS} = 0 V; V_{DS} = 0 V to 480 V [c]	-	260	-	
Total gate charge	Q_g	V_{GS} = 10 V; I_D = 38 A, V_{DS} = 480 V, see fig. 6 and 13 [b]	-	-	330	nC
Gate-source charge	Q_{gs}		-	-	84	
Gate-drain charge	Q_{gd}		-	-	150	
Turn-on delay time	$t_{d(on)}$	V_{GS} = 10 V; V_{DD} = 300 V, I_D = 38 A, R_G = 4.3 Ω, see fig. 10 [b]	-	47	-	ns
Rise time	t_r		-	110	-	
Turn-off delay time	$t_{d(off)}$		-	97	-	
Fall time	t_f		-	60	-	
Drain-source body diode characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	40	A
Pulsed diode forward current [a]	I_{SM}		-	-	160	
Body diode voltage	V_{SD}	T_J = 25 °C, I_S = 38 A, V_{GS} = 0 V [b]	-	-	1.5	V
Body diode reverse recovery time	t_{rr}	T_J = 25 °C; I_F = 38 A, dI/dt = 100 A/μs	-	630	950	ns
		T_J = 125 °C	-	730	1090	
Body diode reverse recovery charge	Q_{rr}	T_J = 25 °C	-	14	20	μC
		T_J = 125 °C	-	17	25	
Body diode recovery current	I_{RRM}	T_J = 25 °C	-	39	58	A
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %

c. C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

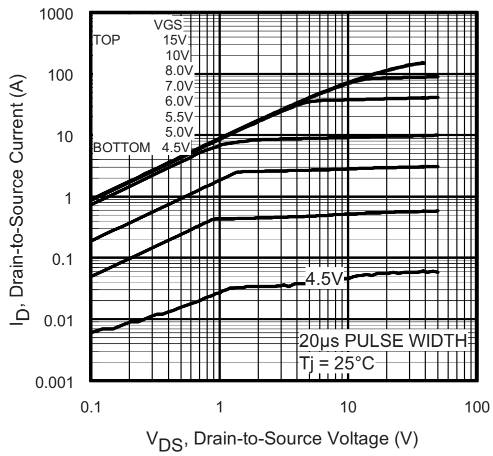


Fig. 1 - Typical Output Characteristics

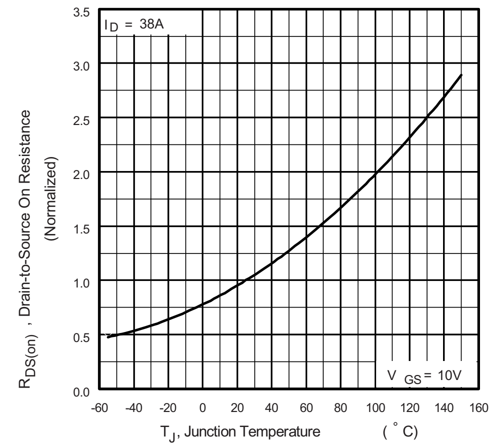


Fig. 4 - Normalized On-Resistance vs. Temperature

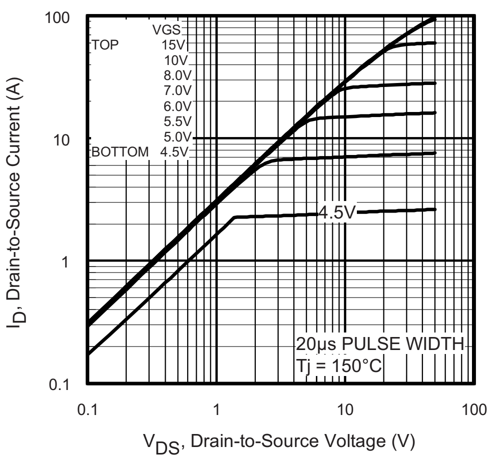


Fig. 2 - Typical Output Characteristics

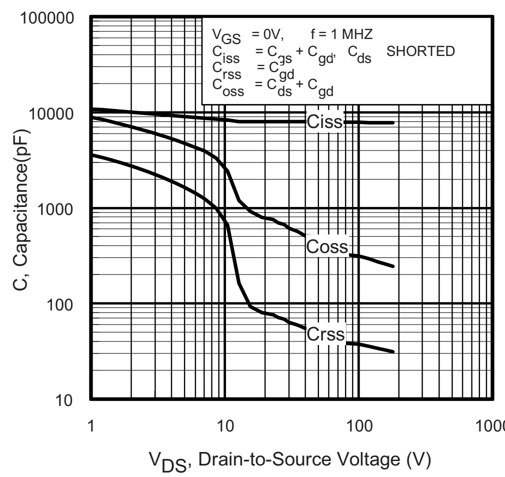


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

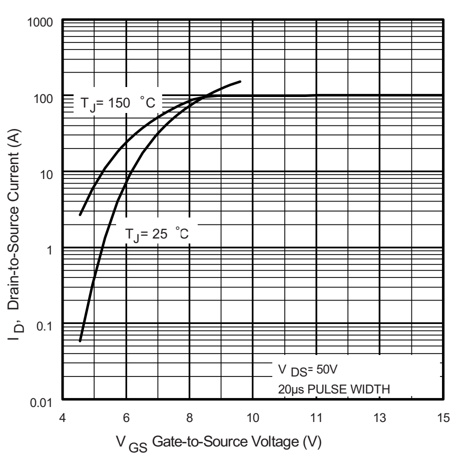


Fig. 3 - Typical Transfer Characteristics

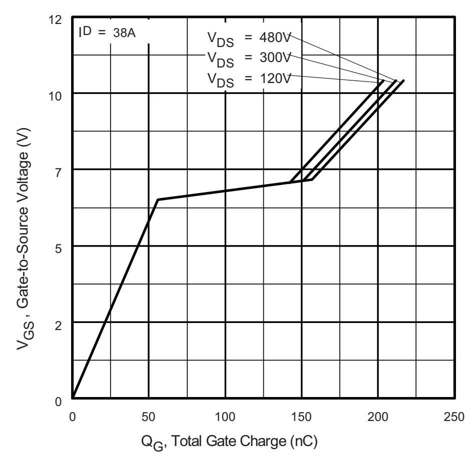


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

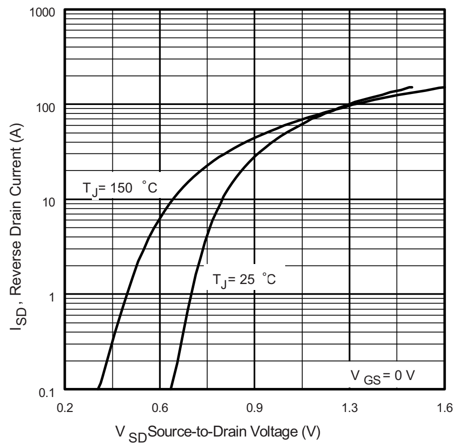


Fig. 7 - Typical Source-Drain Diode Forward Voltage

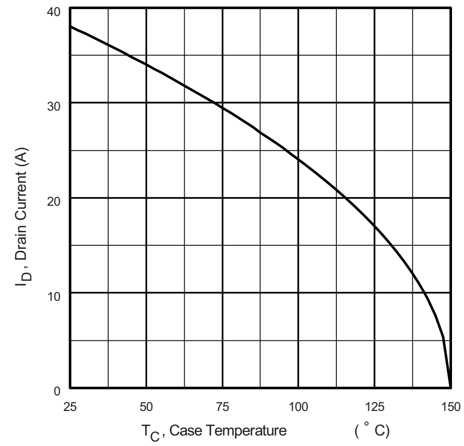


Fig. 9 - Maximum Drain Current vs. Case Temperature

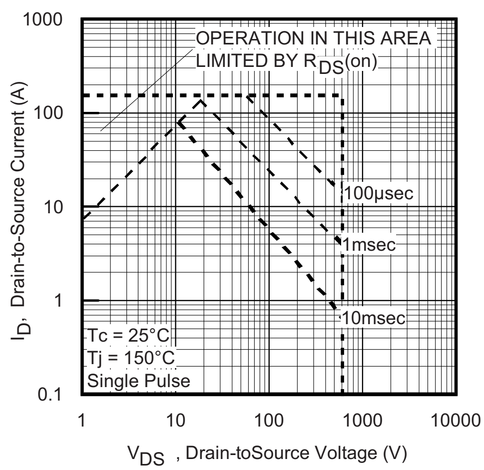


Fig. 8 - Maximum Safe Operating Area

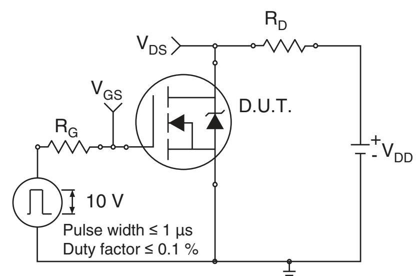


Fig. 10a - Switching Time Test Circuit

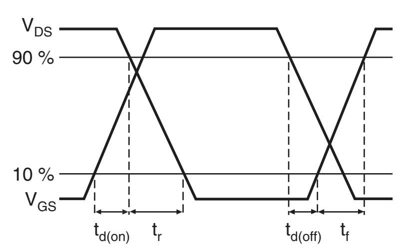


Fig. 10b - Switching Time Waveforms

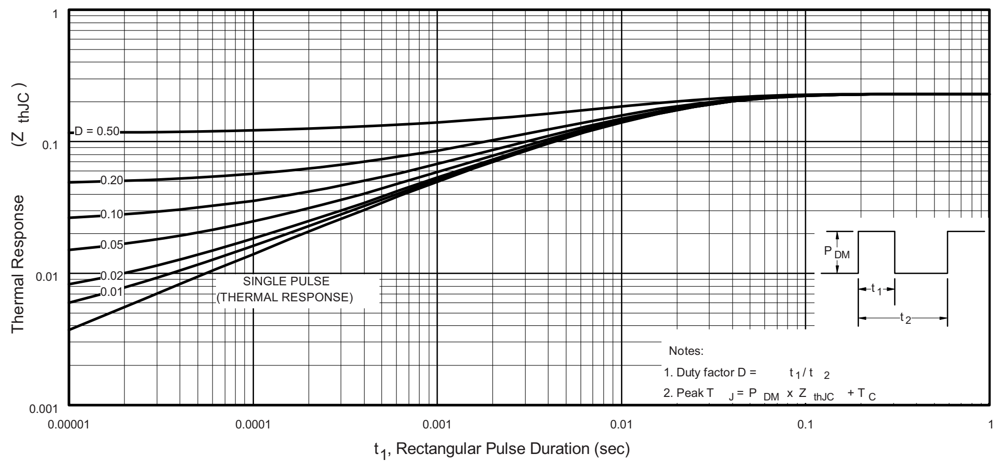


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

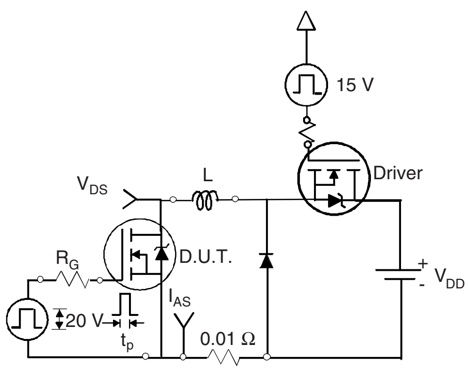


Fig. 12a - Unclamped Inductive Test Circuit

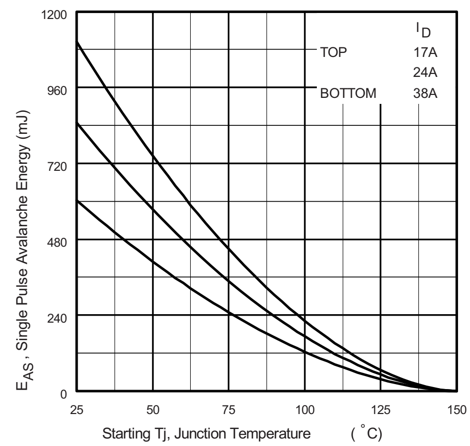


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

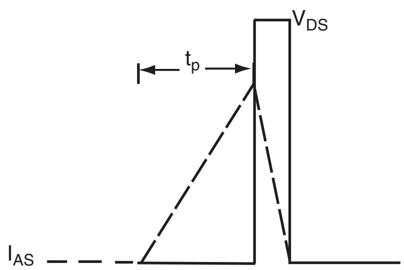


Fig. 12b - Unclamped Inductive Waveforms

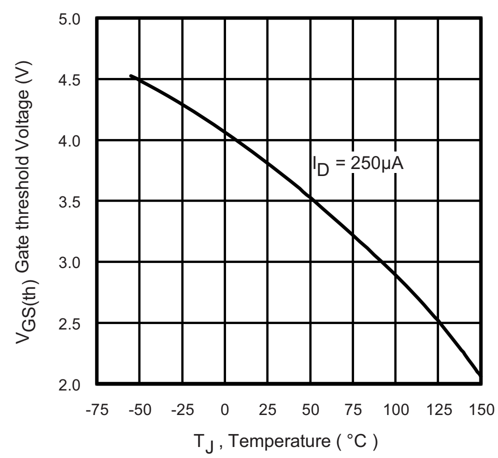


Fig. 12d - Threshold Voltage vs. Temperature

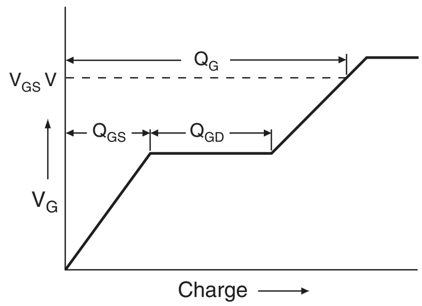


Fig. 13a - Basic Gate Charge Waveform

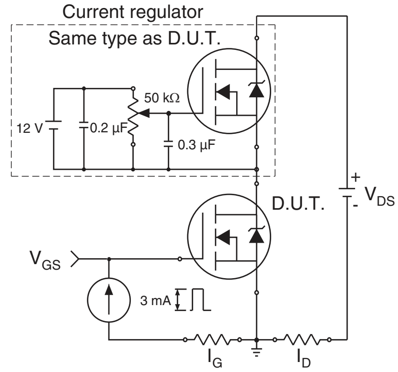
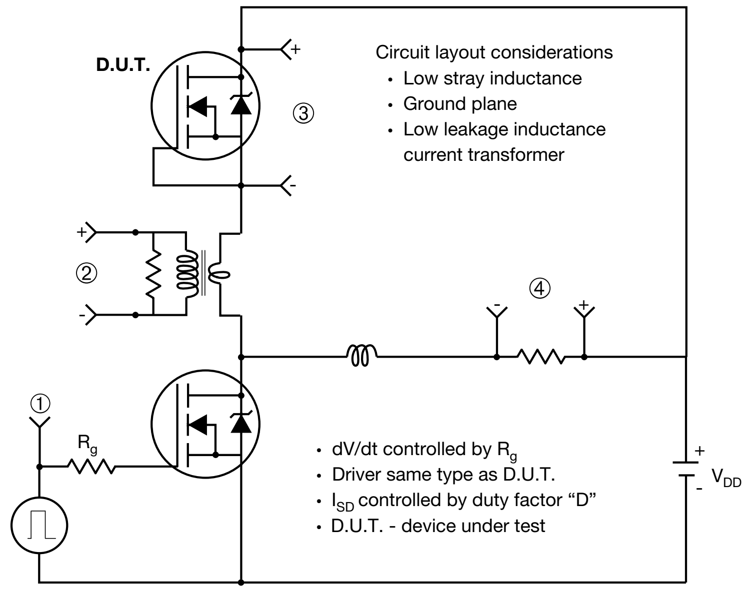
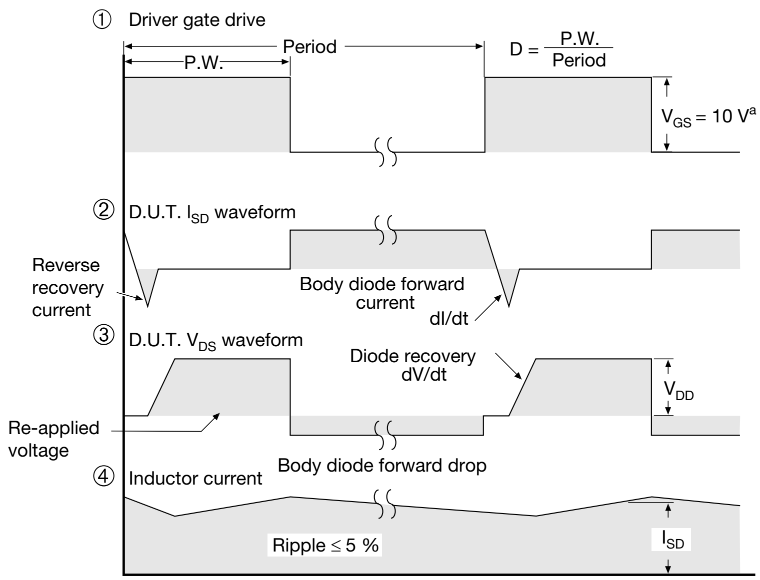


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





Note

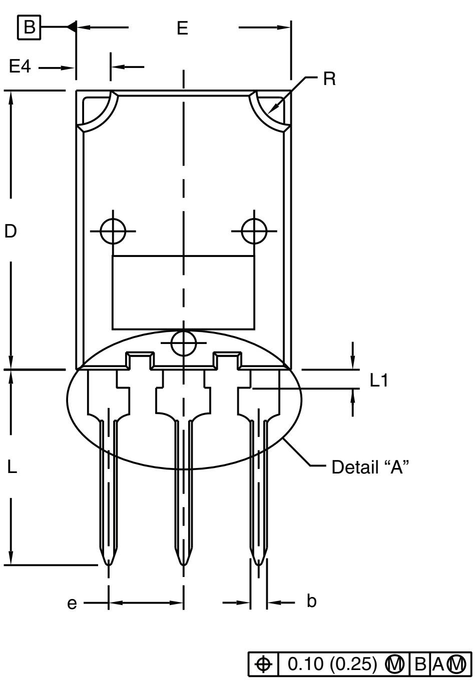
a. V_{GS} = 5 V for logic level devices

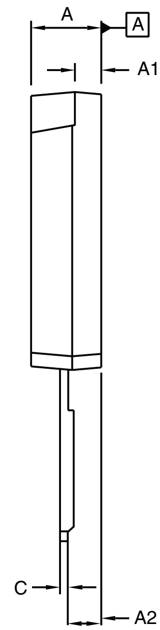
Fig. 14 - For N-Channel

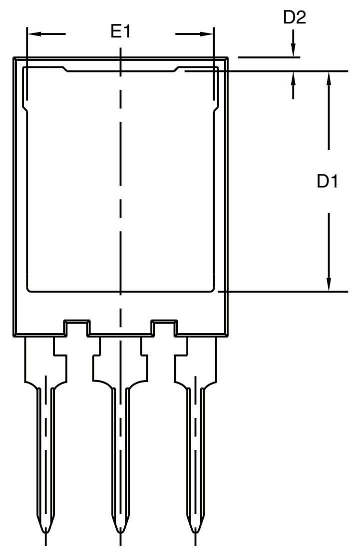
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91261.

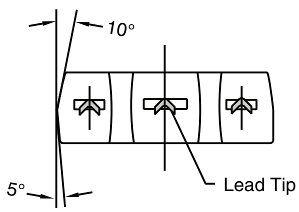
TO-274AA (High Voltage)

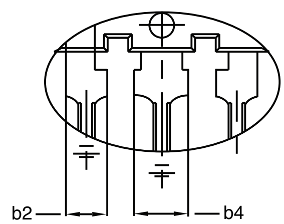
VERSION 1: FACILITY CODE = Y











Detail "A"
Scale: 2:1

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.70	5.30	0.185	0.209
A1	1.50	2.50	0.059	0.098
A2	2.25	2.65	0.089	0.104
b	1.30	1.60	0.051	0.063
b2	1.80	2.20	0.071	0.087
b4	3.00	3.25	0.118	0.128
c [(1)]	0.38	0.89	0.015	0.035
D	19.80	20.80	0.780	0.819

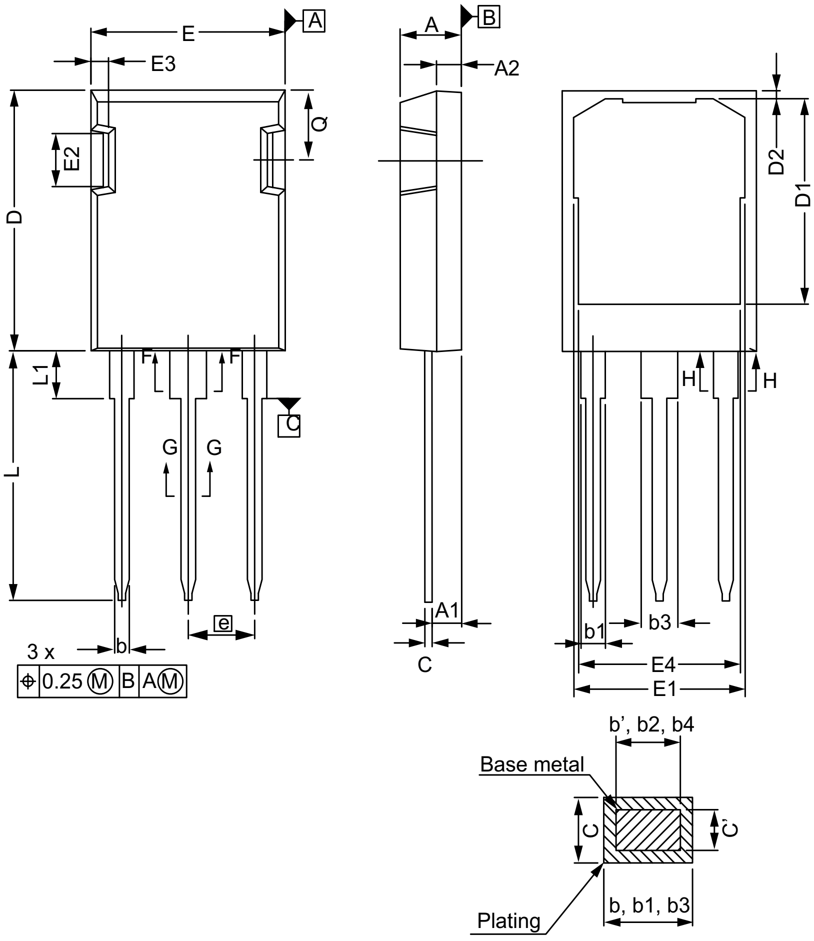
	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	15.50	16.10	0.610	0.634
D2	0.70	1.30	0.028	0.051
E	15.10	16.10	0.594	0.634
E1	13.30	13.90	0.524	0.547
e	5.45 BSC		0.215 BSC	
L	13.70	14.70	0.539	0.579
L1	1.00	1.60	0.039	0.063
R	2.00	3.00	0.079	0.118

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outer extremes of the plastic body
- Outline conforms to JEDEC® outline to TO-274AA

(1) Dimension measured at tip of lead

VERSION 2: FACILITY CODE = N



	MILLIMETERS			MILLIMETERS	
DIM.	MIN.	MAX.	DIM.	MIN.	MAX.
A	4.83	5.21	D1	16.25	17.65
A1	2.29	2.54	D2	0.50	0.80
A2	1.91	2.16	E	15.75	16.13
b'	1.07	1.28	E1	13.10	14.15
b	1.07	1.33	E2	3.68	5.10
b1	1.91	2.41	E3	1.00	1.90
b2	1.91	2.16	E4	12.38	13.43
b3	2.87	3.38	e	5.44 BSC	
b4	2.87	3.13	N	3	
c'	0.55	0.65	L	19.81	20.32
c	0.55	0.68	L1	3.70	4.00
D	20.80	21.10	Q	5.49	6.00

ECN: E20-0538-Rev. C, 19-Oct-2020
DWG: 5975

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Outline conforms to JEDEC® outline to TO-274AD
- Dimensions are measured in mm, angles are in degree
- Metal surfaces are tin plated, except area of cut

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