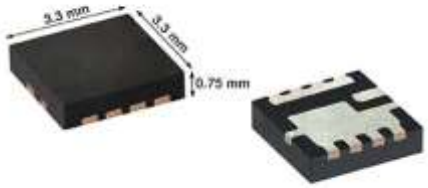
SiSD5300DN 30 V N-Channel MOSFET With Source Flip Technology Delivers High Power Density and Improved Thermal Performance With $R_{DS(ON)}$ Down to 0.71 mΩ and FOM of 42 mΩ*nC in 3.3 mm x 3.3 mm PowerPAK® 1212-F Package With Center Gate Design

Product Benefits:

- Features source flip technology in the 3.3 mm by 3.3 mm PowerPAK 1212-F package
- Best in class on-resistance: 0.71 mΩ at 10 V
- Best in class on-resistance times gate charge FOM of 42 mΩ*nC
- Low thermal resistance of 56 °C/W
- 100 % R_G- and UIS-tested
- RoHS-compliant, and halogen-free



Market Applications:

- Secondary rectification, active clamp, battery management systems (BMS), buck and BLDC converters, OR-ing FETs, motor drives, and load switches for welding equipment and power tools; servers, edge devices, supercomputers, and tablets; lawnmowers and cleaning robots; and radio base stations

The News:

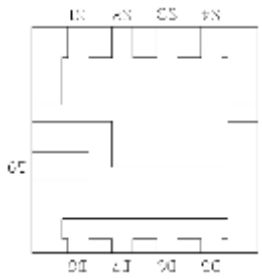
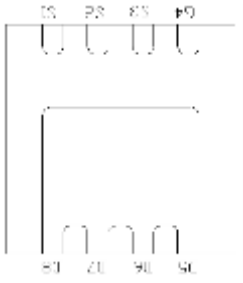
Vishay Intertechnology introduces a versatile new 30 V n-channel TrenchFET® Gen V power MOSFET that delivers increased power density and enhanced thermal performance for industrial, computer, consumer, and telecom applications.

- Occupying the same footprint as the PowerPAK 1212-8S, the SiSD5300DN offers 18 % lower on-resistance to increase power density, while its source flip technology reduces thermal resistance from 63 °C/W to 56 °C/W
- The device's FOM represents a 35 % improvement over previous-generation devices, which translates into reduced conduction and switching losses to save energy in power conversion applications
- PowerPAK1212-F source flip technology reverses the usual proportions of the ground and source pads, extending the area of the ground pad to provide a more efficient thermal dissipation path and thus promoting cooler operation. At the same time, the PowerPAK 1212-F minimizes the extent of the switching area, which helps to reduce the impact of trace noise
- In the PowerPAK 1212-F package specifically, the source pad dimension increases by a factor of 10, from 0.36mm^ to 4.13mm^, enabling a commensurate improvement in thermal performance
- The PowerPAK1212-F's center gate design also simplifies parallelization of multiple devices on a single-layer PCB
- On a 1 in x 1 in FR4, 2-layer PCB with 3 W power dissipation (following the general layout concept) the PowerPAK1212-F has a 15 ˚C lower temperature than the PowerPAK1212-8S

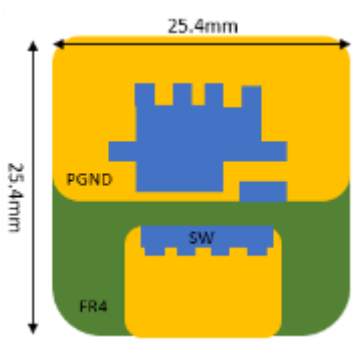
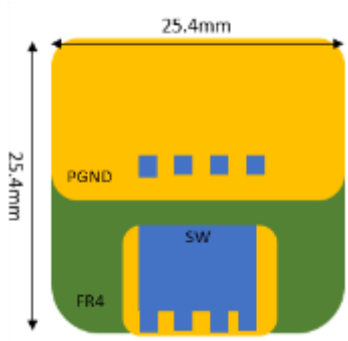
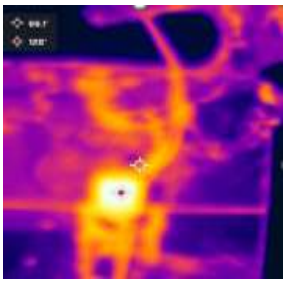
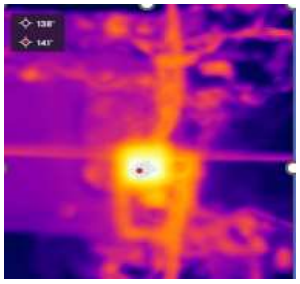
The Key Specifications:

- Package: PowerPAK 1212-F
- Drain-source voltage: 30 V
- Typical on-resistance:
  - At V_{GS} = 10 V: 0.71 mΩ
  - At V_{GS} = 4.5 V: 1.05 mΩ
- Maximum on-resistance:
  - At V_{GS} = 10 V: 0.87 mΩ
  - At V_{GS} = 4.5 V: 1.30 mΩ
- Typical gate charge:
  - At V_{GS} = 10 V: 59 nC
  - At V_{GS} = 4.5 V: 27 nC
- Maximum gate charge:
  - At V_{GS} = 10 V: 36.2 nC
  - At V_{GS} = 4.5 V: 17.6 nC

Package Comparison Table:

PowerPAK1212-F	**PowerPAK1212-8S**
Package size: 3.3 mm x 3.3 mm	Package size: 3.3 mm x 3.3 mm
Thickness : 0.75mm	Thickness : 0.75mm
Source pad dimension: 4.13 mm^	Source pad dimension: 0.36 mm^
Thermal resistance: 56 °C/W	Thermal resistance: 63 °C/W
Lowest available on-resistance in Gen V technology: SiSD5300DN: 0.87 mΩ (maximum)	Lowest available on-resistance in Gen V technology: SiSS54DN: 1.06 mΩ (maximum)
	

Thermal Comparison Table:

PowerPAK1212-F	**PowerPAK1212-8S**
PCB size: 25.4 mm x 25.4 mm	PCB size: 25.4 mm x 25.4 mm
2-layer FR4, 1 oz copper	2-layer FR4, 1 oz copper
Power dissipation: 3 W	Power dissipation: 3 W
Layout concept: Min. switch note (SW) Max. power GND (PGND)	Layout concept: Min. switch note (SW) Max. power GND (PGND)
	
@ PD 3 W: 126 °C 	@ PD 3 W: 141 °C 

Availability:
Samples and production quantities of the SiSD5300DN are available now, with lead times of 26 weeks.

To access the product datasheet on the Vishay Website, go to
http://www.vishay.com/ppg?62220 (SiSD5300DN)

Contact Information:

The Americas
Vishay Americas
LVM_Americas@vishay.com

Europe
Vishay Electronic GmbH
LVM_Europe@vishay.com

Asia
Vishay Intertechnology Asia Pte Ltd.
LVM_Asia@vishay.com